# MAX 7000

## Programmable Logic Device Family

October 2001, ver. 6.2 Data Sheet

## Features...

- High-performance, EEPROM-based programmable logic devices (PLDs) based on second-generation MAX® architecture
- 5.0-V in-system programmability (ISP) through the built-in IEEE Std. 1149.1 Joint Test Action Group (JTAG) interface available in MAX 7000S devices
  - ISP circuitry compatible with IEEE Std. 1532
- Includes 5.0-V MAX 7000 devices and 5.0-V ISP-based MAX 7000S devices
- Built-in JTAG boundary-scan test (BST) circuitry in MAX 7000S devices with 128 or more macrocells
- Complete EPLD family with logic densities ranging from 600 to 5,000 usable gates (see Tables 1 and 2)
- 5-ns pin-to-pin logic delays with up to 175.4-MHz counter frequencies (including interconnect)
- PCI-compliant devices available

For information on in-system programmable 3.3-V MAX 7000A or 2.5-V MAX 7000B devices, see the *MAX 7000A Programmable Logic Device Family Data Sheet* or the *MAX 7000B Programmable Logic Device Family Data Sheet*.

*Table 1. MAX 7000 Device Features*

| Feature | EPM7032 | EPM7064 | EPM7096 | EPM7128E | EPM7160E | EPM7192E | EPM7256E |
|---|---|---|---|---|---|---|---|
| Usable gates | 600 | 1,250 | 1,800 | 2,500 | 3,200 | 3,750 | 5,000 |
| Macrocells | 32 | 64 | 96 | 128 | 160 | 192 | 256 |
| Logic array blocks | 2 | 4 | 6 | 8 | 10 | 12 | 16 |
| Maximum user I/O pins | 36 | 68 | 76 | 100 | 104 | 124 | 164 |
| $t_{PD}$ (ns) | 6 | 6 | 7.5 | 7.5 | 10 | 12 | 12 |
| $t_{SU}$ (ns) | 5 | 5 | 6 | 6 | 7 | 7 | 7 |
| $t_{FSU}$ (ns) | 2.5 | 2.5 | 3 | 3 | 3 | 3 | 3 |
| $t_{CO1}$ (ns) | 4 | 4 | 4.5 | 4.5 | 5 | 6 | 6 |
| $f_{CNT}$ (MHz) | 151.5 | 151.5 | 125.0 | 125.0 | 100.0 | 90.9 | 90.9 |

*Table 2. MAX 7000S Device Features*

| Feature | EPM7032S | EPM7064S | EPM7128S | EPM7160S | EPM7192S | EPM7256S |
|---|---|---|---|---|---|---|
| Usable gates | 600 | 1,250 | 2,500 | 3,200 | 3,750 | 5,000 |
| Macrocells | 32 | 64 | 128 | 160 | 192 | 256 |
| Logic array blocks | 2 | 4 | 8 | 10 | 12 | 16 |
| Maximum user I/O pins | 36 | 68 | 100 | 104 | 124 | 164 |
| $t_{PD}$ (ns) | 5 | 5 | 6 | 6 | 7.5 | 7.5 |
| $t_{SU}$ (ns) | 2.9 | 2.9 | 3.4 | 3.4 | 4.1 | 3.9 |
| $t_{FSU}$ (ns) | 2.5 | 2.5 | 2.5 | 2.5 | 3 | 3 |
| $t_{CO1}$ (ns) | 3.2 | 3.2 | 4 | 3.9 | 4.7 | 4.7 |
| $f_{CNT}$ (MHz) | 175.4 | 175.4 | 147.1 | 149.3 | 125.0 | 128.2 |

## …and More Features

- Open-drain output option in MAX 7000S devices
- Programmable macrocell flipflops with individual clear, preset, clock, and clock enable controls
- Programmable power-saving mode for a reduction of over 50% in each macrocell
- Configurable expander product-term distribution, allowing up to 32 product terms per macrocell
- 44 to 208 pins available in plastic J-lead chip carrier (PLCC), ceramic pin-grid array (PGA), plastic quad flat pack (PQFP), power quad flat pack (RQFP), and 1.0-mm thin quad flat pack (TQFP) packages
- Programmable security bit for protection of proprietary designs
- 3.3-V or 5.0-V operation
  - MultiVolt™ I/O interface operation, allowing devices to interface with 3.3-V or 5.0-V devices (MultiVolt I/O operation is not available in 44-pin packages)
  - Pin compatible with low-voltage MAX 7000A and MAX 7000B devices
- Enhanced features available in MAX 7000E and MAX 7000S devices
  - Six pin- or logic-driven output enable signals
  - Two global clock signals with optional inversion
  - Enhanced interconnect resources for improved routability
  - Fast input setup times provided by a dedicated path from I/O pin to macrocell registers
  - Programmable output slew-rate control
- Software design support and automatic place-and-route provided by Altera's development system for Windows-based PCs and Sun SPARCstation, and HP 9000 Series 700/800 workstations

- Additional design entry and simulation support provided by EDIF 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPM), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, and VeriBest
- Programming support
  - Altera's Master Programming Unit (MPU) and programming hardware from third-party manufacturers program all MAX 7000 devices
  - The BitBlaster™ serial download cable, ByteBlasterMV™ parallel port download cable, and MasterBlaster™ serial/universal serial bus (USB) download cable program MAX 7000S devices

## General Description

The MAX 7000 family of high-density, high-performance PLDs is based on Altera's second-generation MAX architecture. Fabricated with advanced CMOS technology, the EEPROM-based MAX 7000 family provides 600 to 5,000 usable gates, ISP, pin-to-pin delays as fast as 5 ns, and counter speeds of up to 175.4 MHz. MAX 7000S devices in the -5, -6, -7, and -10 speed grades as well as MAX 7000 and MAX 7000E devices in -5, -6, -7, -10P, and -12P speed grades comply with the PCI Special Interest Group (PCI SIG) ***PCI Local Bus Specification, Revision 2.2***. See Table 3 for available speed grades.

*Table 3. MAX 7000 Speed Grades*

| Device | Speed Grade | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | -5 | -6 | -7 | -10P | -10 | -12P | -12 | -15 | -15T | -20 |
| EPM7032 | | ✓ | ✓ | | ✓ | | ✓ | ✓ | ✓ | |
| EPM7032S | ✓ | ✓ | ✓ | | ✓ | | | | | |
| EPM7064 | | ✓ | ✓ | | ✓ | | ✓ | ✓ | | |
| EPM7064S | ✓ | ✓ | ✓ | | ✓ | | | | | |
| EPM7096 | | | ✓ | | ✓ | | ✓ | ✓ | | |
| EPM7128E | | | ✓ | ✓ | ✓ | | ✓ | ✓ | | ✓ |
| EPM7128S | | ✓ | ✓ | | ✓ | | | ✓ | | |
| EPM7160E | | | | ✓ | ✓ | | ✓ | ✓ | | ✓ |
| EPM7160S | | ✓ | ✓ | | ✓ | | | ✓ | | |
| EPM7192E | | | | | | ✓ | ✓ | ✓ | | ✓ |
| EPM7192S | | | ✓ | | ✓ | | | ✓ | | |
| EPM7256E | | | | | | ✓ | ✓ | ✓ | | ✓ |
| EPM7256S | | | ✓ | | ✓ | | | ✓ | | |

The MAX 7000E devices—including the EPM7128E, EPM7160E, EPM7192E, and EPM7256E devices—have several enhanced features: additional global clocking, additional output enable controls, enhanced interconnect resources, fast input registers, and a programmable slew rate.

In-system programmable MAX 7000 devices—called MAX 7000S devices—include the EPM7032S, EPM7064S, EPM7128S, EPM7160S, EPM7192S, and EPM7256S devices. MAX 7000S devices have the enhanced features of MAX 7000E devices as well as JTAG BST circuitry in devices with 128 or more macrocells, ISP, and an open-drain output option. See Table 4.

*Table 4. MAX 7000 Device Features*

| Feature | EPM7032 EPM7064 EPM7096 | All MAX 7000E Devices | All MAX 7000S Devices |
|---|---|---|---|
| ISP via JTAG interface | | | ✓ |
| JTAG BST circuitry | | | ✓ *(1)* |
| Open-drain output option | | | ✓ |
| Fast input registers | | ✓ | ✓ |
| Six global output enables | | ✓ | ✓ |
| Two global clocks | | ✓ | ✓ |
| Slew-rate control | | ✓ | ✓ |
| MultiVolt interface *(2)* | ✓ | ✓ | ✓ |
| Programmable register | ✓ | ✓ | ✓ |
| Parallel expanders | ✓ | ✓ | ✓ |
| Shared expanders | ✓ | ✓ | ✓ |
| Power-saving mode | ✓ | ✓ | ✓ |
| Security bit | ✓ | ✓ | ✓ |
| PCI-compliant devices available | ✓ | ✓ | ✓ |

*Notes:*
(1) Available only in EPM7128S, EPM7160S, EPM7192S, and EPM7256S devices only.
(2) The MultiVolt I/O interface is not available in 44-pin packages.

The MAX 7000 architecture supports 100% TTL emulation and high-density integration of SSI, MSI, and LSI logic functions. The MAX 7000 architecture easily integrates multiple devices ranging from PALs, GALs, and 22V10s to MACH and pLSI devices. MAX 7000 devices are available in a wide range of packages, including PLCC, PGA, PQFP, RQFP, and TQFP packages. See Table 5.

*Table 5. MAX 7000 Maximum User I/O Pins* *Note (1)*

| Device | 44-Pin PLCC | 44-Pin PQFP | 44-Pin TQFP | 68-Pin PLCC | 84-Pin PLCC | 100-Pin PQFP | 100-Pin TQFP | 160-Pin PQFP | 160-Pin PGA | 192-Pin PGA | 208-Pin PQFP | 208-Pin RQFP |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| EPM7032 | 36 | 36 | 36 | | | | | | | | | |
| EPM7032S | 36 | | 36 | | | | | | | | | |
| EPM7064 | 36 | | 36 | 52 | 68 | 68 | | | | | | |
| EPM7064S | 36 | | 36 | | 68 | | 68 | | | | | |
| EPM7096 | | | | 52 | 64 | 76 | | | | | | |
| EPM7128E | | | | | 68 | 84 | | 100 | | | | |
| EPM7128S | | | | | 68 | 84 | 84 *(2)* | 100 | | | | |
| EPM7160E | | | | | 64 | 84 | | 104 | | | | |
| EPM7160S | | | | | 64 | | 84 *(2)* | 104 | | | | |
| EPM7192E | | | | | | | | 124 | 124 | | | |
| EPM7192S | | | | | | | | 124 | | | | |
| EPM7256E | | | | | | | | 132 *(2)* | | 164 | | 164 |
| EPM7256S | | | | | | | | | | | 164 *(2)* | 164 |

*Notes:*

(1) When the JTAG interface in MAX 7000S devices is used for either boundary-scan testing or for ISP, four I/O pins become JTAG pins.

(2) Perform a complete thermal analysis before committing a design to this device package. For more information, see the *Operating Requirements for Altera Devices Data Sheet*.

MAX 7000 devices use CMOS EEPROM cells to implement logic functions. The user-configurable MAX 7000 architecture accommodates a variety of independent combinatorial and sequential logic functions. The devices can be reprogrammed for quick and efficient iterations during design development and debug cycles, and can be programmed and erased up to 100 times.

MAX 7000 devices contain from 32 to 256 macrocells that are combined into groups of 16 macrocells, called logic array blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register with independently programmable clock, clock enable, clear, and preset functions. To build complex logic functions, each macrocell can be supplemented with both shareable expander product terms and high-speed parallel expander product terms to provide up to 32 product terms per macrocell.

The MAX 7000 family provides programmable speed/power optimization. Speed-critical portions of a design can run at high speed/full power, while the remaining portions run at reduced speed/low power. This speed/power optimization feature enables the designer to configure one or more macrocells to operate at 50% or lower power while adding only a nominal timing delay. MAX 7000E and MAX 7000S devices also provide an option that reduces the slew rate of the output buffers, minimizing noise transients when non-speed-critical signals are switching. The output drivers of all MAX 7000 devices (except 44-pin devices) can be set for either 3.3-V or 5.0-V operation, allowing MAX 7000 devices to be used in mixed-voltage systems.

The MAX 7000 family is supported by Altera development systems, which are integrated packages that offer schematic, text—including VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL)—and waveform design entry, compilation and logic synthesis, simulation and timing analysis, and device programming. The software provides EDIF 2 0 0 and 3 0 0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX-workstation-based EDA tools. The software runs on Windows-based PCs, as well as Sun SPARCstation, and HP 9000 Series 700/800 workstations.

For more information on development tools, see the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* and the *Quartus Programmable Logic Development System & Software Data Sheet*.

## Functional Description

The MAX 7000 architecture includes the following elements:

- Logic array blocks
- Macrocells
- Expander product terms (shareable and parallel)
- Programmable interconnect array
- I/O control blocks

The MAX 7000 architecture includes four dedicated inputs that can be used as general-purpose inputs or as high-speed, global control signals (clock, clear, and two output enable signals) for each macrocell and I/O pin. Figure 1 shows the architecture of EPM7032, EPM7064, and EPM7096 devices.

*Figure 1. EPM7032, EPM7064 & EPM7096 Device Block Diagram*

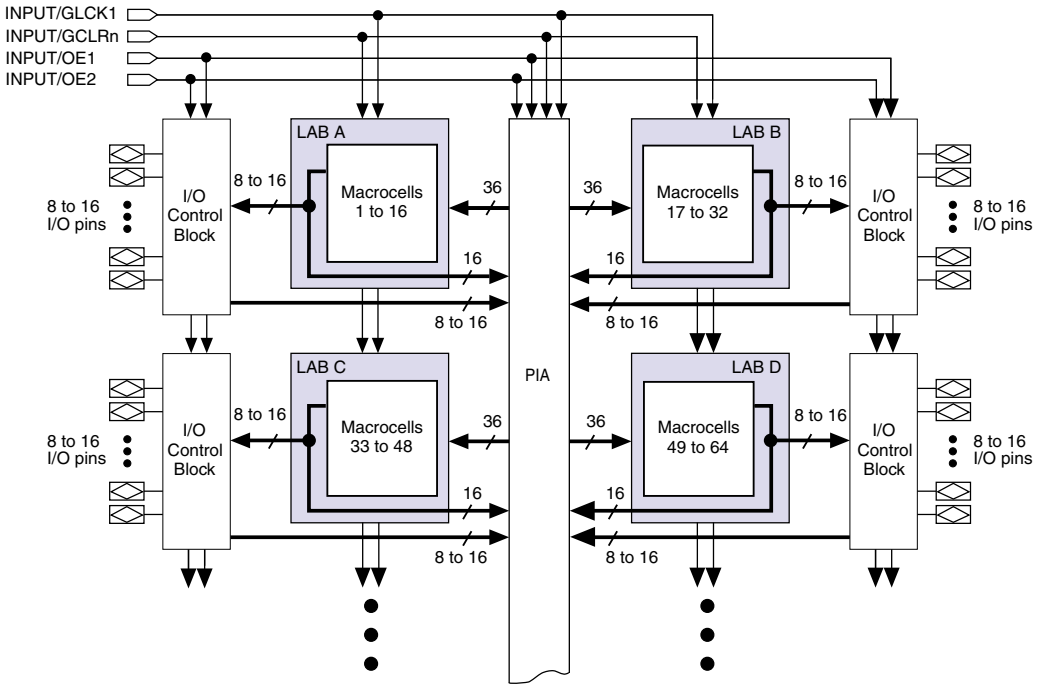
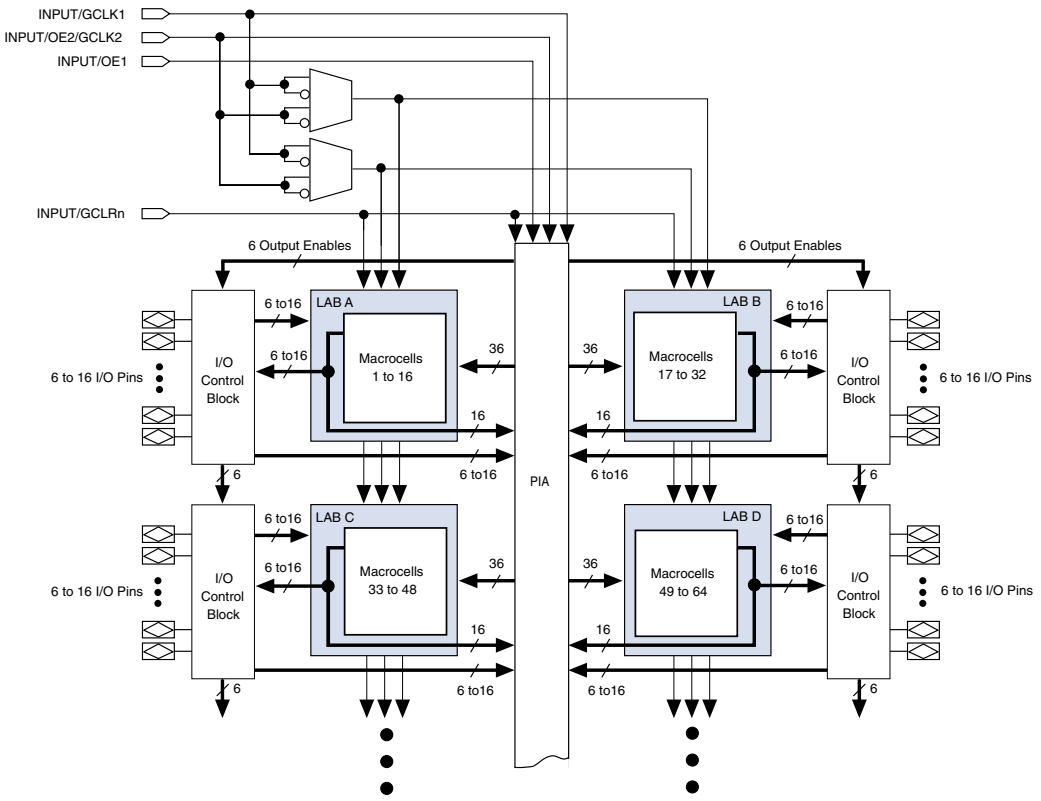


Figure 2 shows the architecture of MAX 7000E and MAX 7000S devices.

*Figure 2. MAX 7000E & MAX 7000S Device Block Diagram*




## Logic Array Blocks

The MAX 7000 device architecture is based on the linking of high-performance, flexible, logic array modules called logic array blocks (LABs). LABs consist of 16-macrocell arrays, as shown in Figures 1 and 2. Multiple LABs are linked together via the programmable interconnect array (PIA), a global bus that is fed by all dedicated inputs, I/O pins, and macrocells.

Each LAB is fed by the following signals:

- 36 signals from the PIA that are used for general logic inputs
- Global controls that are used for secondary register functions
- Direct input paths from I/O pins to the registers that are used for fast setup times for MAX 7000E and MAX 7000S devices

## Macrocells

The MAX 7000 macrocell can be individually configured for either sequential or combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term select matrix, and the programmable register. The macrocell of EPM7032, EPM7064, and EPM7096 devices is shown in Figure 3.

*Figure 3. EPM7032, EPM7064 & EPM7096 Device Macrocell*

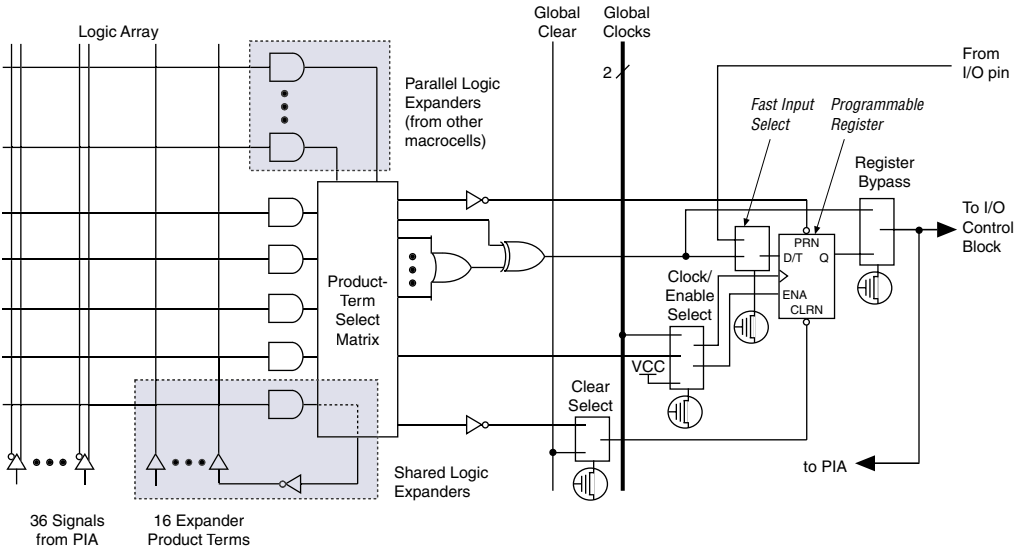
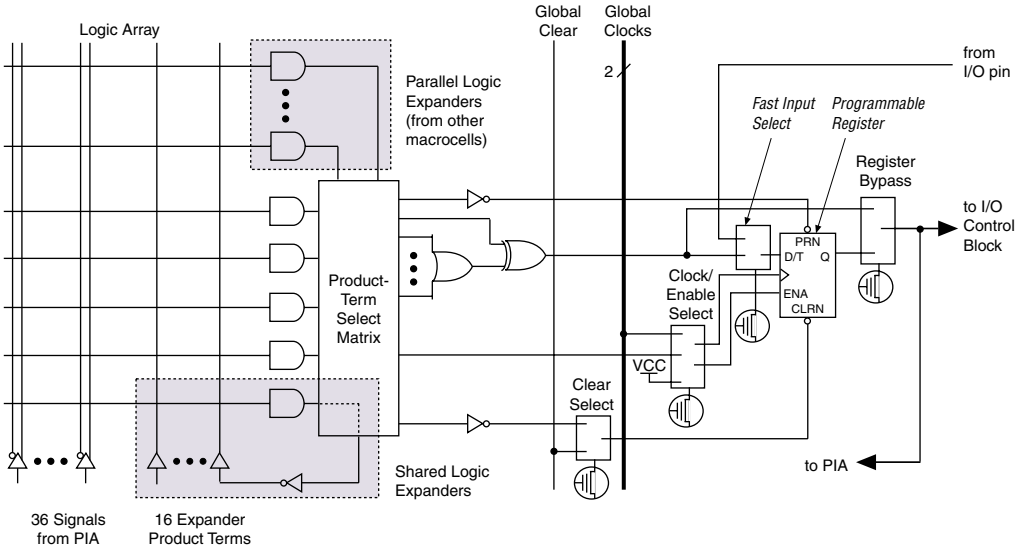


Figure 4 shows a MAX 7000E and MAX 7000S device macrocell.

*Figure 4. MAX 7000E & MAX 7000S Device Macrocell*




Combinatorial logic is implemented in the logic array, which provides five product terms per macrocell. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as secondary inputs to the macrocell's register clear, preset, clock, and clock enable control functions. Two kinds of expander product terms ("expanders") are available to supplement macrocell logic resources:

- Shareable expanders, which are inverted product terms that are fed back into the logic array
- Parallel expanders, which are product terms borrowed from adjacent macrocells

The Altera development system automatically optimizes product-term allocation according to the logic requirements of the design.

For registered functions, each macrocell flipflop can be individually programmed to implement D, T, JK, or SR operation with programmable clock control. The flipflop can be bypassed for combinatorial operation. During design entry, the designer specifies the desired flipflop type; the Altera development software then selects the most efficient flipflop operation for each registered function to optimize resource utilization.

Each programmable register can be clocked in three different modes:

- By a global clock signal. This mode achieves the fastest clock-to-output performance.
- By a global clock signal and enabled by an active-high clock enable. This mode provides an enable on each flipflop while still achieving the fast clock-to-output performance of the global clock.
- By an array clock implemented with a product term. In this mode, the flipflop can be clocked by signals from buried macrocells or I/O pins.

In EPM7032, EPM7064, and EPM7096 devices, the global clock signal is available from a dedicated clock pin, `GCLK1`, as shown in Figure 1. In MAX 7000E and MAX 7000S devices, two global clock signals are available. As shown in Figure 2, these global clock signals can be the true or the complement of either of the global clock pins, `GCLK1` or `GCLK2`.

Each register also supports asynchronous preset and clear functions. As shown in Figures 3 and 4, the product-term select matrix allocates product terms to control these operations. Although the product-term-driven preset and clear of the register are active high, active-low control can be obtained by inverting the signal within the logic array. In addition, each register clear function can be individually driven by the active-low dedicated global clear pin (`GCLRn`). Upon power-up, each register in the device will be set to a low state.

All MAX 7000E and MAX 7000S I/O pins have a fast input path to a macrocell register. This dedicated path allows a signal to bypass the PIA and combinatorial logic and be driven to an input D flipflop with an extremely fast (2.5 ns) input setup time.

## Expander Product Terms

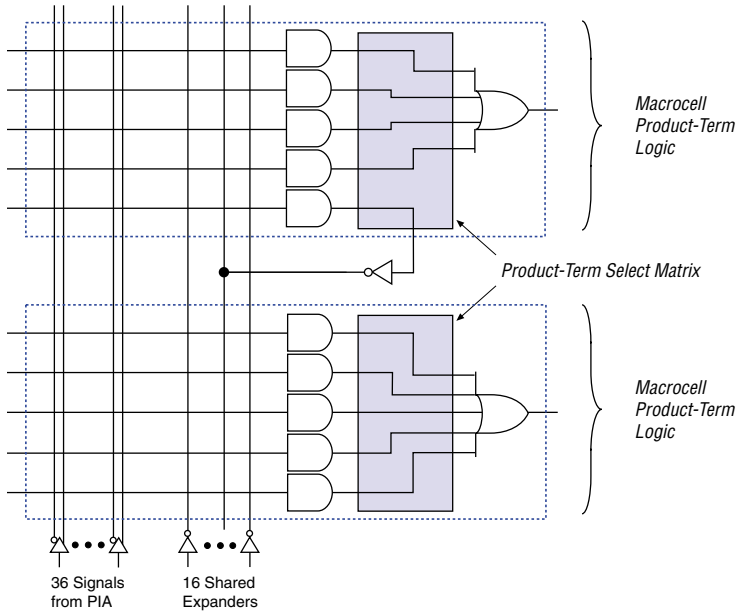
Although most logic functions can be implemented with the five product terms available in each macrocell, the more complex logic functions require additional product terms. Another macrocell can be used to supply the required logic resources; however, the MAX 7000 architecture also allows both shareable and parallel expander product terms (“expanders”) that provide additional product terms directly to any macrocell in the same LAB. These expanders help ensure that logic is synthesized with the fewest possible logic resources to obtain the fastest possible speed.

### Shareable Expanders

Each LAB has 16 shareable expanders that can be viewed as a pool of uncommitted single product terms (one from each macrocell) with inverted outputs that feed back into the logic array. Each shareable expander can be used and shared by any or all macrocells in the LAB to build complex logic functions. A small delay ($t_{SEXP}$) is incurred when shareable expanders are used. Figure 5 shows how shareable expanders can feed multiple macrocells.

**Figure 5. Shareable Expanders**

*Shareable expanders can be shared by any or all macrocells in an LAB.*




### Parallel Expanders

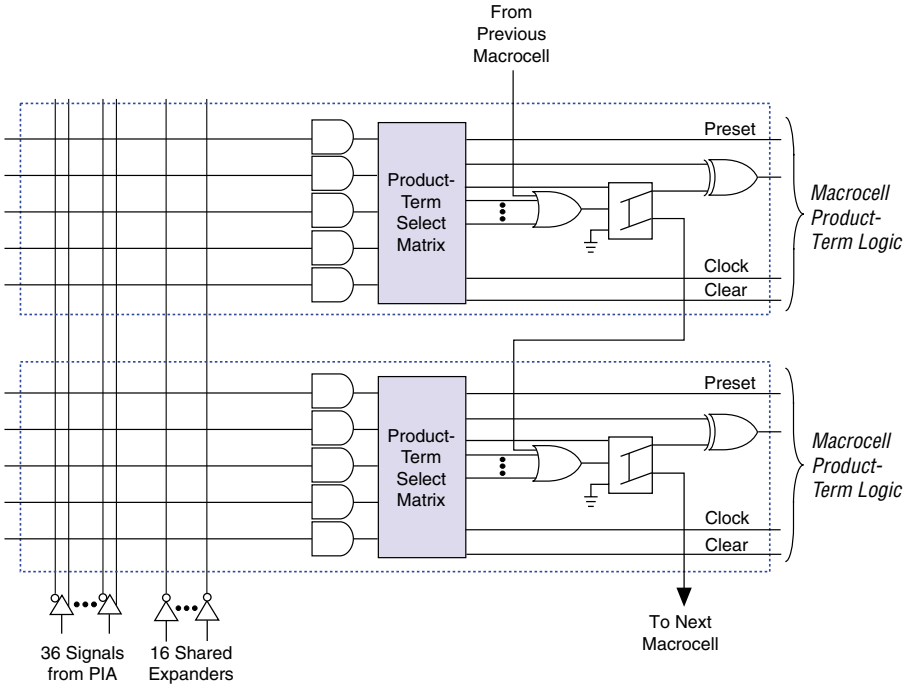
Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with five product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB.

The compiler can allocate up to three sets of up to five parallel expanders automatically to the macrocells that require additional product terms. Each set of five parallel expanders incurs a small, incremental timing delay ($t_{PEXP}$). For example, if a macrocell requires 14 product terms, the Compiler uses the five dedicated product terms within the macrocell and allocates two sets of parallel expanders; the first set includes five product terms and the second set includes four product terms, increasing the total delay by 2 × $t_{PEXP}$.

Two groups of 8 macrocells within each LAB (e.g., macrocells 1 through 8 and 9 through 16) form two chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of 8, the lowest-numbered macrocell can only lend parallel expanders and the highest-numbered macrocell can only borrow them. Figure 6 shows how parallel expanders can be borrowed from a neighboring macrocell.

***Figure 6. Parallel Expanders***

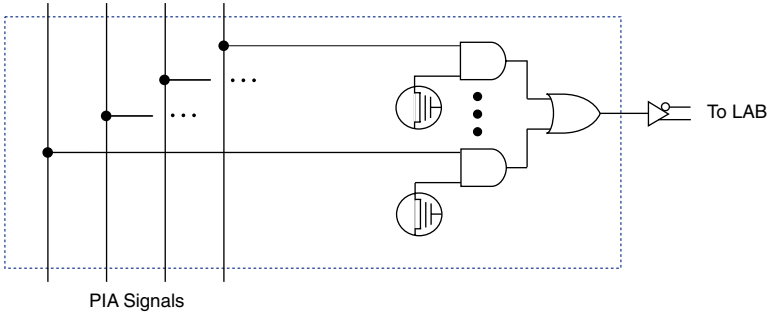
*Unused product terms in a macrocell can be allocated to a neighboring macrocell.*



## Programmable Interconnect Array

Logic is routed between LABs via the programmable interconnect array (PIA). This global bus is a programmable path that connects any signal source to any destination on the device. All MAX 7000 dedicated inputs, I/O pins, and macrocell outputs feed the PIA, which makes the signals available throughout the entire device. Only the signals required by each LAB are actually routed from the PIA into the LAB. Figure 7 shows how the PIA signals are routed into the LAB. An EEPROM cell controls one input to a 2-input AND gate, which selects a PIA signal to drive into the LAB.

*Figure 7. PIA Routing*



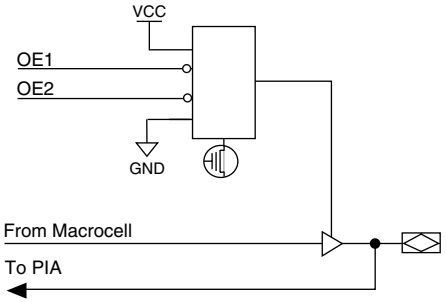

While the routing delays of channel-based routing schemes in masked or FPGAs are cumulative, variable, and path-dependent, the MAX 7000 PIA has a fixed delay. The PIA thus eliminates skew between signals and makes timing performance easy to predict.

## I/O Control Blocks

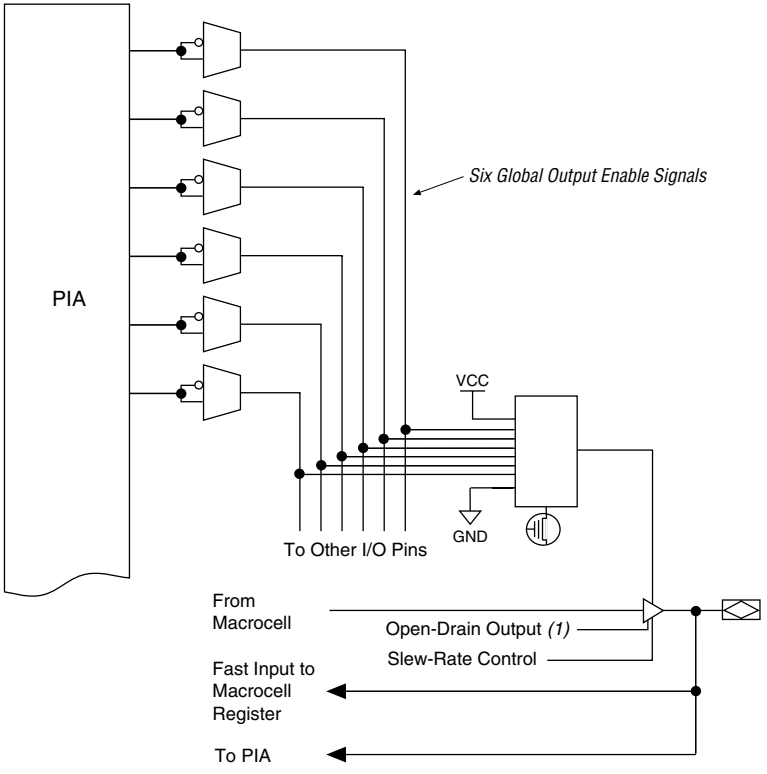
The I/O control block allows each I/O pin to be individually configured for input, output, or bidirectional operation. All I/O pins have a tri-state buffer that is individually controlled by one of the global output enable signals or directly connected to ground or $V_{CC}$. Figure 8 shows the I/O control block for the MAX 7000 family. The I/O control block of EPM7032, EPM7064, and EPM7096 devices has two global output enable signals that are driven by two dedicated active-low output enable pins (OE1 and OE2). The I/O control block of MAX 7000E and MAX 7000S devices has six global output enable signals that are driven by the true or complement of two output enable signals, a subset of the I/O pins, or a subset of the I/O macrocells.

*Figure 8. I/O Control Block of MAX 7000 Devices*

**EPM7032, EPM7064 & EPM7096 Devices**




**MAX 7000E & MAX 7000S Devices**




*Note:*
(1) The open-drain output option is available only in MAX 7000S devices.

When the tri-state buffer control is connected to ground, the output is tri-stated (high impedance) and the I/O pin can be used as a dedicated input. When the tri-state buffer control is connected to $V_{CC}$, the output is enabled.

The MAX 7000 architecture provides dual I/O feedback, in which macrocell and pin feedbacks are independent. When an I/O pin is configured as an input, the associated macrocell can be used for buried logic.

## In-System Programmability (ISP)

MAX 7000S devices are in-system programmable via an industry-standard 4-pin Joint Test Action Group (JTAG) interface (IEEE Std. 1149.1-1990). ISP allows quick, efficient iterations during design development and debugging cycles. The MAX 7000S architecture internally generates the high programming voltage required to program EEPROM cells, allowing in-system programming with only a single 5.0 V power supply. During in-system programming, the I/O pins are tri-stated and pulled-up to eliminate board conflicts. The pull-up value is nominally 50 kΩ.

ISP simplifies the manufacturing flow by allowing devices to be mounted on a printed circuit board with standard in-circuit test equipment before they are programmed. MAX 7000S devices can be programmed by downloading the information via in-circuit testers (ICT), embedded processors, or the Altera MasterBlaster, ByteBlasterMV, ByteBlaster, BitBlaster download cables. (The ByteBlaster cable is obsolete and is replaced by the ByteBlasterMV cable, which can program and configure 2.5-V, 3.3-V, and 5.0-V devices.) Programming the devices after they are placed on the board eliminates lead damage on high-pin-count packages (e.g., QFP packages) due to device handling and allows devices to be reprogrammed after a system has already shipped to the field. For example, product upgrades can be performed in the field via software or modem.

In-system programming can be accomplished with either an adaptive or constant algorithm. An adaptive algorithm reads information from the unit and adapts subsequent programming steps to achieve the fastest possible programming time for that unit. Because some in-circuit testers cannot support an adaptive algorithm, Altera offers devices tested with a constant algorithm. Devices tested to the constant algorithm are marked with an "F" suffix in the ordering code.

The Jam™ Standard Test and Programming Language (STAPL) can be used to program MAX 7000S devices with in-circuit testers, PCs, or embedded processor.

For more information on using the Jam language, see *Application Note 88 (Using the Jam Language for ISP & ICR via an Embedded Processor)*.

The ISP circuitry in MAX 7000S devices is compatible with IEEE Std. 1532 specification. The IEEE Std. 1532 is a standard developed to allow concurrent ISP between multiple PLD vendors.

## Programmable Speed/Power Control

MAX 7000 devices offer a power-saving mode that supports low-power operation across user-defined signal paths or the entire device. This feature allows total power dissipation to be reduced by 50% or more, because most logic applications require only a small fraction of all gates to operate at maximum frequency.

The designer can program each individual macrocell in a MAX 7000 device for either high-speed (i.e., with the Turbo Bit™ option turned on) or low-power (i.e., with the Turbo Bit option turned off) operation. As a result, speed-critical paths in the design can run at high speed, while the remaining paths can operate at reduced power. Macrocells that run at low power incur a nominal timing delay adder ($t_{LPA}$) for the $t_{LAD}$, $t_{LAC}$, $t_{IC}$, $t_{EN}$, and $t_{SEXP}$, $\mathbf{t_{ACL}}$, and $\mathbf{t_{CPPW}}$ parameters.

## Output Configuration

MAX 7000 device outputs can be programmed to meet a variety of system-level requirements.

### MultiVolt I/O Interface

MAX 7000 devices—except 44-pin devices—support the MultiVolt I/O interface feature, which allows MAX 7000 devices to interface with systems that have differing supply voltages. The 5.0-V devices in all packages can be set for 3.3-V or 5.0-V I/O pin operation. These devices have one set of `VCC` pins for internal operation and input buffers (`VCCINT`), and another set for I/O output drivers (`VCCIO`).

The `VCCINT` pins must always be connected to a 5.0-V power supply. With a 5.0-V $V_{CCINT}$ level, input voltage thresholds are at TTL levels, and are therefore compatible with both 3.3-V and 5.0-V inputs.

The `VCCIO` pins can be connected to either a 3.3-V or a 5.0-V power supply, depending on the output requirements. When the `VCCIO` pins are connected to a 5.0-V supply, the output levels are compatible with 5.0-V systems. When $V_{CCIO}$ is connected to a 3.3-V supply, the output high is 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with $V_{CCIO}$ levels lower than 4.75 V incur a nominally greater timing delay of $t_{OD2}$ instead of $t_{OD1}$.

### Open-Drain Output Option (MAX 7000S Devices Only)

MAX 7000S devices provide an optional open-drain (functionally equivalent to open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. It can also provide an additional wired-OR plane.

Output pins on 5.0-V MAX 7000S devices with $V_{CCIO}$ = 3.3 V or 5.0 V (with a pull-up resistor to the 5.0-V supply) can also drive 5.0-V CMOS input pins. In this case, the pull-up transistor will turn off when the pin voltage exceeds 3.3 V. Therefore, the pin does not have to be open-drain.

### Slew-Rate Control

The output buffer for each MAX 7000E and MAX 7000S I/O pin has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay of 4 to 5 ns. In MAX 7000E devices, when the Turbo Bit is turned off, the slew rate is set for low noise performance. For MAX 7000S devices, each I/O pin has an individual EEPROM bit that controls the slew rate, allowing designers to specify the slew rate on a pin-by-pin basis.

## Programming with External Hardware

MAX 7000 devices can be programmed on Windows-based PCs with the Altera Logic Programmer card, the Master Programming Unit (MPU), and the appropriate device adapter. The MPU performs a continuity check to ensure adequate electrical contact between the adapter and the device.

For more information, see the *Altera Programming Hardware Data Sheet*.

The Altera development system can use text- or waveform-format test vectors created with the Text Editor or Waveform Editor to test the programmed device. For added design verification, designers can perform functional testing to compare the functional behavior of a MAX 7000 device with the results of simulation. Moreover, Data I/O, BP Microsystems, and other programming hardware manufacturers also provide programming support for Altera devices.

For more information, see the *Programming Hardware Manufacturers*.

## IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

MAX 7000 devices support JTAG BST circuitry as specified by IEEE Std. 1149.1-1990. Table 6 describes the JTAG instructions supported by the MAX 7000 family. The pin-out tables (see the Altera web site (**http://www.altera.com**) or the *Altera Digital Library* for pin-out information) show the location of the JTAG control pins for each device. If the JTAG interface is not required, the JTAG pins are available as user I/O pins.

*Table 6. MAX 7000 JTAG Instructions*

| JTAG Instruction | Devices | Description |
|---|---|---|
| SAMPLE/PRELOAD | EPM7128S<br>EPM7160S<br>EPM7192S<br>EPM7256S | Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern output at the device pins. |
| EXTEST | EPM7128S<br>EPM7160S<br>EPM7192S<br>EPM7256S | Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins. |
| BYPASS | EPM7032S<br>EPM7064S<br>EPM7128S<br>EPM7160S<br>EPM7192S<br>EPM7256S | Places the 1-bit bypass register between the `TDI` and `TDO` pins, which allows the BST data to pass synchronously through a selected device to adjacent devices during normal device operation. |
| IDCODE | EPM7032S<br>EPM7064S<br>EPM7128S<br>EPM7160S<br>EPM7192S<br>EPM7256S | Selects the IDCODE register and places it between `TDI` and `TDO`, allowing the IDCODE to be serially shifted out of `TDO`. |
| ISP Instructions | EPM7032S<br>EPM7064S<br>EPM7128S<br>EPM7160S<br>EPM7192S<br>EPM7256S | These instructions are used when programming MAX 7000S devices via the JTAG ports with the MasterBlaster, ByteBlasterMV, BitBlaster download cable, or using a Jam File (**.jam**), Jam Byte-Code file (**.jbc**), or Serial Vector Format file (**.svf**) via an embedded processor or test equipment. |

The instruction register length of MAX 7000S devices is 10 bits. Tables 7 and 8 show the boundary-scan register length and device IDCODE information for MAX 7000S devices.

*Table 7. MAX 7000S Boundary-Scan Register Length*

| Device | Boundary-Scan Register Length |
|---|---|
| EPM7032S | 1 *(1)* |
| EPM7064S | 1 *(1)* |
| EPM7128S | 288 |
| EPM7160S | 312 |
| EPM7192S | 360 |
| EPM7256S | 480 |

*Note:*
(1) This device does not support JTAG boundary-scan testing. Selecting either the EXTEST or SAMPLE/PRELOAD instruction will select the one-bit bypass register.

*Table 8. 32-Bit MAX 7000 Device IDCODE* *Note (1)*

| Device | IDCODE (32 Bits) | | | |
|---|---|---|---|---|
| | Version (4 Bits) | Part Number (16 Bits) | Manufacturer's Identity (11 Bits) | 1 (1 Bit) *(2)* |
| EPM7032S | 0000 | 0111 0000 0011 0010 | 00001101110 | 1 |
| EPM7064S | 0000 | 0111 0000 0110 0100 | 00001101110 | 1 |
| EPM7128S | 0000 | 0111 0001 0010 1000 | 00001101110 | 1 |
| EPM7160S | 0000 | 0111 0001 0110 0000 | 00001101110 | 1 |
| EPM7192S | 0000 | 0111 0001 1001 0010 | 00001101110 | 1 |
| EPM7256S | 0000 | 0111 0010 0101 0110 | 00001101110 | 1 |

*Notes:*
(1) The most significant bit (MSB) is on the left.
(2) The least significant bit (LSB) for all JTAG IDCODEs is 1.

Figure 9 shows the timing requirements for the JTAG signals.

*Figure 9. MAX 7000 JTAG Waveforms*

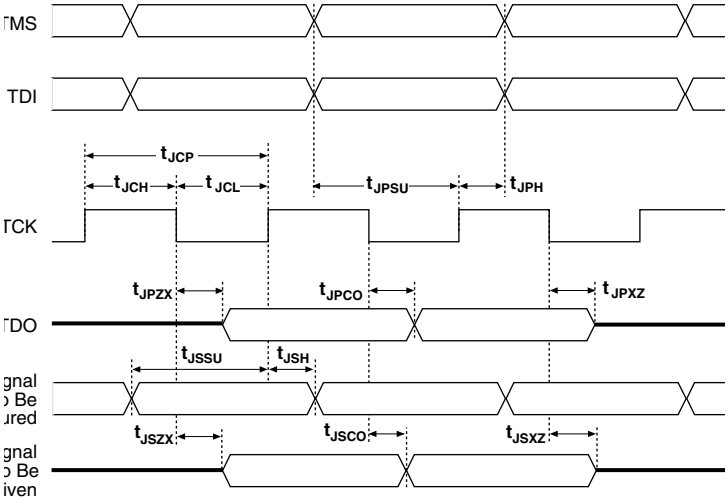



Table 9 shows the JTAG timing parameters and values for MAX 7000S devices.

*Table 9. JTAG Timing Parameters & Values for MAX 7000S Devices*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{JCP}$ | TCK clock period | 100 | | ns |
| $t_{JCH}$ | TCK clock high time | 50 | | ns |
| $t_{JCL}$ | TCK clock low time | 50 | | ns |
| $t_{JPSU}$ | JTAG port setup time | 20 | | ns |
| $t_{JPH}$ | JTAG port hold time | 45 | | ns |
| $t_{JPCO}$ | JTAG port clock to output | | 25 | ns |
| $t_{JPZX}$ | JTAG port high impedance to valid output | | 25 | ns |
| $t_{JPXZ}$ | JTAG port valid output to high impedance | | 25 | ns |
| $t_{JSSU}$ | Capture register setup time | 20 | | ns |
| $t_{JSH}$ | Capture register hold time | 45 | | ns |
| $t_{JSCO}$ | Update register clock to output | | 25 | ns |
| $t_{JSZX}$ | Update register high impedance to valid output | | 25 | ns |
| $t_{JSXZ}$ | Update register valid output to high impedance | | 25 | ns |

For more information, see *Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*.

## Design Security

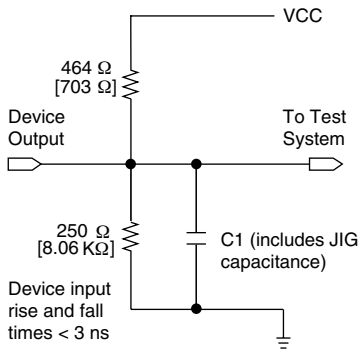
All MAX 7000 devices contain a programmable security bit that controls access to the data programmed into the device. When this bit is programmed, a proprietary design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security because programmed data within EEPROM cells is invisible. The security bit that controls this function, as well as all other programmed data, is reset only when the device is reprogrammed.

## Generic Testing

Each MAX 7000 device is functionally tested. Complete testing of each programmable EEPROM bit and all internal logic elements ensures 100% programming yield. AC test measurements are taken under conditions equivalent to those shown in Figure 10. Test patterns can be used and then erased during early stages of the production flow.

***Figure 10. MAX 7000 AC Test Conditions***

*Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in brackets are for 2.5-V devices and outputs. Numbers without brackets are for 3.3-V devices and outputs.*




## QFP Carrier & Development Socket

MAX 7000 and MAX 7000E devices in QFP packages with 100 or more pins are shipped in special plastic carriers to protect the QFP leads. The carrier is used with a prototype development socket and special programming hardware available from Altera. This carrier technology makes it possible to program, test, erase, and reprogram a device without exposing the leads to mechanical stress.

For detailed information and carrier dimensions, refer to the *QFP Carrier & Development Socket Data Sheet*.

MAX 7000S devices are not shipped in carriers.

## Operating Conditions

Tables 10 through 15 provide information about absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for 5.0-V MAX 7000 devices.

*Table 10. MAX 7000 5.0-V Device Absolute Maximum Ratings* *Note (1)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to ground *(2)* | –2.0 | 7.0 | V |
| $V_I$ | DC input voltage | | –2.0 | 7.0 | V |
| $I_{OUT}$ | DC output current, per pin | | –25 | 25 | mA |
| $T_{STG}$ | Storage temperature | No bias | –65 | 150 | ° C |
| $T_{AMB}$ | Ambient temperature | Under bias | –65 | 135 | ° C |
| $T_J$ | Junction temperature | Ceramic packages, under bias | | 150 | ° C |
| | | PQFP and RQFP packages, under bias | | 135 | ° C |

*Table 11. MAX 7000 5.0-V Device Recommended Operating Conditions*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage for internal logic and input buffers | *(3)*, *(4)* | 4.75 (4.50) | 5.25 (5.50) | V |
| $V_{CCIO}$ | Supply voltage for output drivers, 5.0-V operation | *(3)*, *(4)* | 4.75 (4.50) | 5.25 (5.50) | V |
| | Supply voltage for output drivers, 3.3-V operation | *(3)*, *(4)*, *(5)* | 3.00 (3.00) | 3.60 (3.60) | V |
| $V_{CCISP}$ | Supply voltage during ISP | *(6)* | 4.75 | 5.25 | V |
| $V_I$ | Input voltage | | –0.5 *(7)* | $V_{CCINT}$ + 0.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CCIO}$ | V |
| $T_A$ | Ambient temperature | For commercial use | 0 | 70 | ° C |
| | | For industrial use | –40 | 85 | ° C |
| $T_J$ | Junction temperature | For commercial use | 0 | 90 | ° C |
| | | For industrial use | –40 | 105 | ° C |
| $t_R$ | Input rise time | | | 40 | ns |
| $t_F$ | Input fall time | | | 40 | ns |

*Table 12. MAX 7000 5.0-V Device DC Operating Conditions* *Note (8)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | 2.0 | $V_{CCINT}$ + 0.5 | V |
| $V_{IL}$ | Low-level input voltage | | –0.5 *(7)* | 0.8 | V |
| $V_{OH}$ | 5.0-V high-level TTL output voltage | $I_{OH}$ = –4 mA DC, $V_{CCIO}$ = 4.75 V *(9)* | 2.4 | | V |
| | 3.3-V high-level TTL output voltage | $I_{OH}$ = –4 mA DC, $V_{CCIO}$ = 3.00 V *(9)* | 2.4 | | V |
| | 3.3-V high-level CMOS output voltage | $I_{OH}$ = –0.1 mA DC, $V_{CCIO}$ = 3.0 V *(9)* | $V_{CCIO}$ – 0.2 | | V |
| $V_{OL}$ | 5.0-V low-level TTL output voltage | $I_{OL}$ = 12 mA DC, $V_{CCIO}$ = 4.75 V *(10)* | | 0.45 | V |
| | 3.3-V low-level TTL output voltage | $I_{OL}$ = 12 mA DC, $V_{CCIO}$ = 3.00 V *(10)* | | 0.45 | V |
| | 3.3-V low-level CMOS output voltage | $I_{OL}$ = 0.1 mA DC, $V_{CCIO}$ = 3.0 V*(10)* | | 0.2 | V |
| $I_I$ | Leakage current of dedicated input pins | $V_I$ = –0.5 to 5.5 V *(10)* | –10 | 10 | µA |
| $I_{OZ}$ | I/O pin tri-state output off-state current | $V_I$ = –0.5 to 5.5 V *(10)*, *(11)* | –40 | 40 | µA |

*Table 13. MAX 7000 5.0-V Device Capacitance: EPM7032, EPM7064 & EPM7096 Devices* *Note (12)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input pin capacitance | $V_{IN}$ = 0 V, f = 1.0 MHz | | 12 | pF |
| $C_{I/O}$ | I/O pin capacitance | $V_{OUT}$ = 0 V, f = 1.0 MHz | | 12 | pF |

*Table 14. MAX 7000 5.0-V Device Capacitance: MAX 7000E Devices* *Note (12)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input pin capacitance | $V_{IN}$ = 0 V, f = 1.0 MHz | | 15 | pF |
| $C_{I/O}$ | I/O pin capacitance | $V_{OUT}$ = 0 V, f = 1.0 MHz | | 15 | pF |

*Table 15. MAX 7000 5.0-V Device Capacitance: MAX 7000S Devices* *Note (12)*

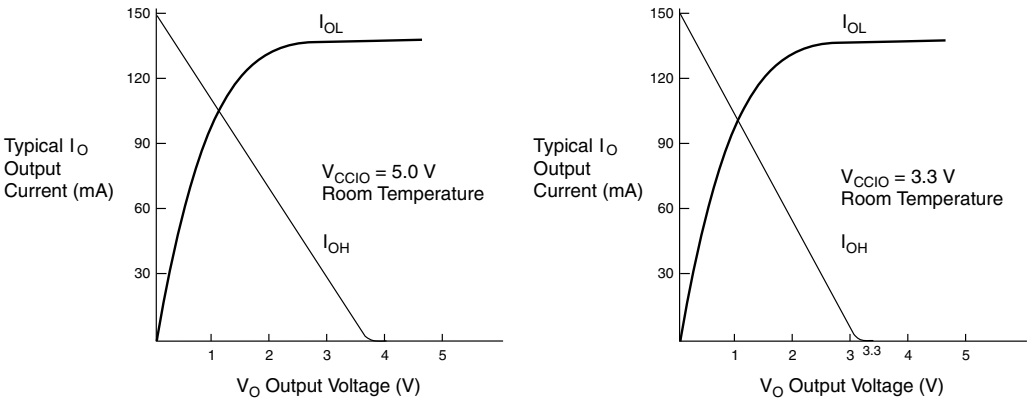
| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Dedicated input pin capacitance | $V_{IN}$ = 0 V, f = 1.0 MHz | | 10 | pF |
| $C_{I/O}$ | I/O pin capacitance | $V_{OUT}$ = 0 V, f = 1.0 MHz | | 10 | pF |

*Notes to tables:*

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC input voltage on I/O pins is –0.5 V and on 4 dedicated input pins is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) Numbers in parentheses are for industrial-temperature-range devices.
(4) $V_{CC}$ must rise monotonically.
(5) 3.3-V I/O operation is not available for 44-pin packages.
(6) The $V_{CCISP}$ parameter applies only to MAX 7000S devices.
(7) During in-system programming, the minimum DC input voltage is –0.3 V.
(8) These values are specified under the MAX 7000 recommended operating conditions in Table 11 on page 23.
(9) The parameter is measured with 50% of the outputs each sourcing the specified current. The $I_{OH}$ parameter refers to high-level TTL or CMOS output current.
(10) The parameter is measured with 50% of the outputs each sinking the specified current. The $I_{OL}$ parameter refers to low-level TTL, PCI, or CMOS output current.
(11) When the JTAG interface is enabled in MAX 7000S devices, the input leakage current on the JTAG pins is typically –60 µA.
(12) Capacitance is measured at 25° C and is sample-tested only. The `OE1` pin has a maximum capacitance of 20 pF.

Figure 11 shows the typical output drive characteristics of MAX 7000 devices.

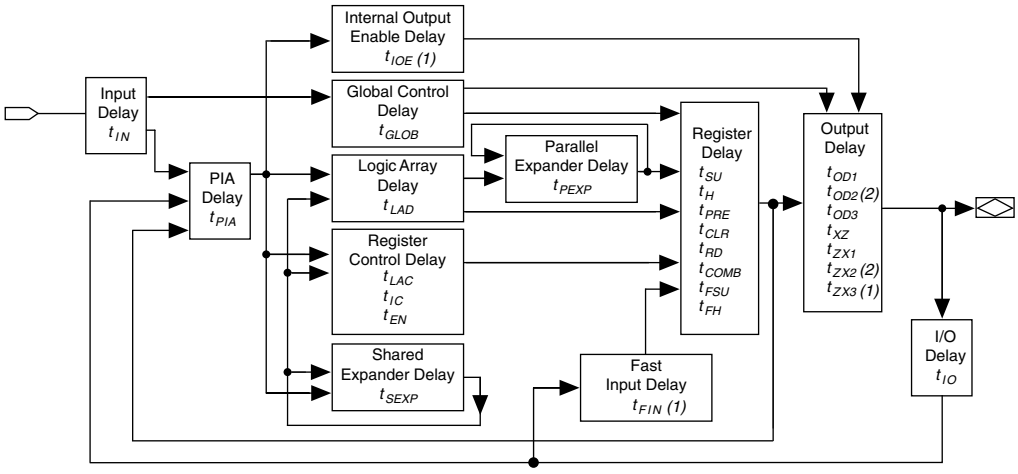
***Figure 11. Output Drive Characteristics of 5.0-V MAX 7000 Devices***




## Timing Model

MAX 7000 device timing can be analyzed with the Altera software, with a variety of popular industry-standard EDA simulators and timing analyzers, or with the timing model shown in Figure 12. MAX 7000 devices have fixed internal delays that enable the designer to determine the worst-case timing of any design. The Altera software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for a device-wide performance evaluation.

*Figure 12. MAX 7000 Timing Model*



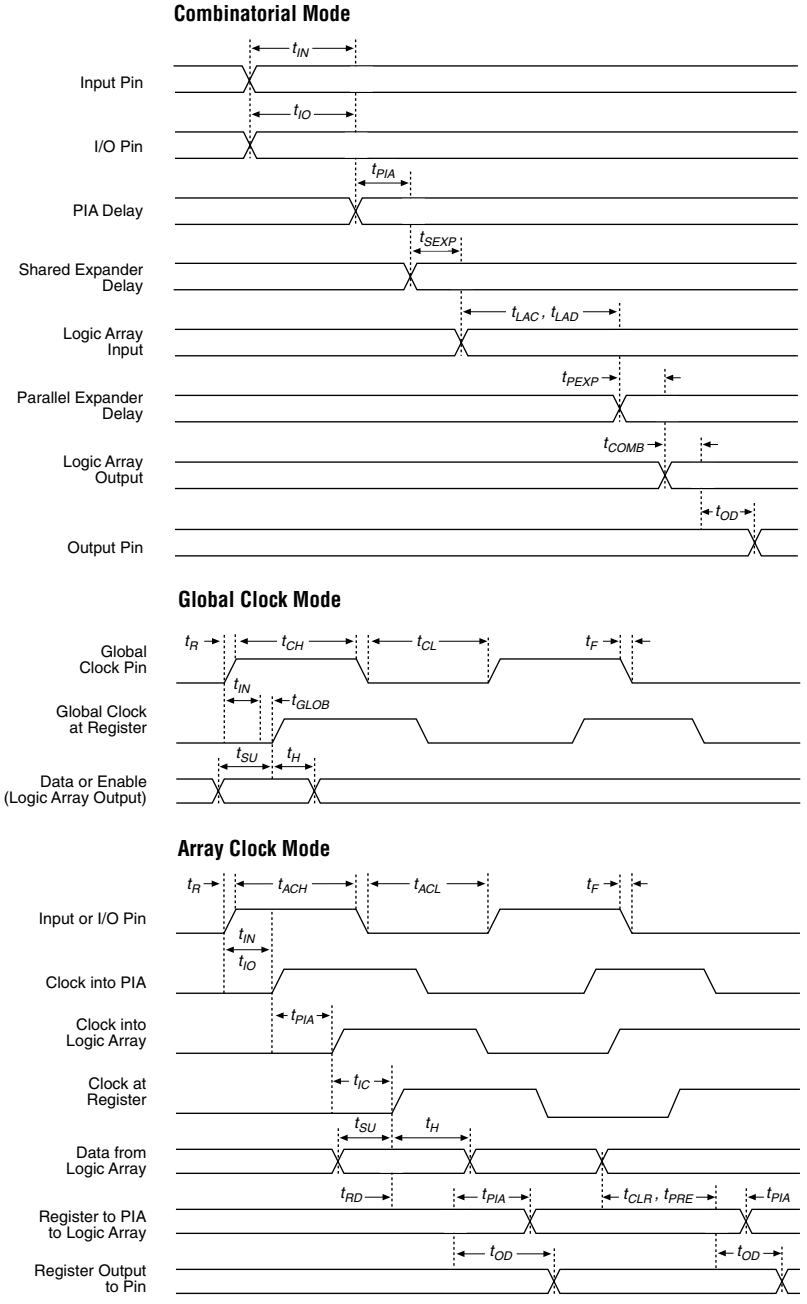

*Notes:*
(1) Only available in MAX 7000E and MAX 7000S devices.
(2) Not available in 44-pin devices.

The timing characteristics of any signal path can be derived from the timing model and parameters of a particular device. External timing parameters, which represent pin-to-pin timing delays, can be calculated as the sum of internal parameters. Figure 13 shows the internal timing relationship of internal and external delay parameters.

For more infomration, see *Application Note 94 (Understanding MAX 7000 Timing)*.

*Figure 13. Switching Waveforms*

*$t_R$ & $t_F$ < 3 ns. Inputs are driven at 3 V for a logic high and 0 V for a logic low. All timing characteristics are measured at 1.5 V.*



Tables 16 through 23 show the MAX 7000 and MAX 7000E AC operating conditions.

**Table 16. MAX 7000 & MAX 7000E External Timing Parameters** *Note (1)*

| Symbol | Parameter | Conditions | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $t_{PD1}$ | Input to non-registered output | C1 = 35 pF | | 6.0 | | 7.5 | ns |
| $t_{PD2}$ | I/O input to non-registered output | C1 = 35 pF | | 6.0 | | 7.5 | ns |
| $t_{SU}$ | Global clock setup time | | 5.0 | | 6.0 | | ns |
| $t_{H}$ | Global clock hold time | | 0.0 | | 0.0 | | ns |
| $t_{FSU}$ | Global clock setup time of fast input | *(2)* | 2.5 | | 3.0 | | ns |
| $t_{FH}$ | Global clock hold time of fast input | *(2)* | 0.5 | | 0.5 | | ns |
| $t_{CO1}$ | Global clock to output delay | C1 = 35 pF | | 4.0 | | 4.5 | ns |
| $t_{CH}$ | Global clock high time | | 2.5 | | 3.0 | | ns |
| $t_{CL}$ | Global clock low time | | 2.5 | | 3.0 | | ns |
| $t_{ASU}$ | Array clock setup time | | 2.5 | | 3.0 | | ns |
| $t_{AH}$ | Array clock hold time | | 2.0 | | 2.0 | | ns |
| $t_{ACO1}$ | Array clock to output delay | C1 = 35 pF | | 6.5 | | 7.5 | ns |
| $t_{ACH}$ | Array clock high time | | 3.0 | | 3.0 | | ns |
| $t_{ACL}$ | Array clock low time | | 3.0 | | 3.0 | | ns |
| $t_{CPPW}$ | Minimum pulse width for clear and preset | *(3)* | 3.0 | | 3.0 | | ns |
| $t_{ODH}$ | Output data hold time after clock | C1 = 35 pF *(4)* | 1.0 | | 1.0 | | ns |
| $t_{CNT}$ | Minimum global clock period | | | 6.6 | | 8.0 | ns |
| $f_{CNT}$ | Maximum internal global clock frequency | *(5)* | 151.5 | | 125.0 | | MHz |
| $t_{ACNT}$ | Minimum array clock period | | | 6.6 | | 8.0 | ns |
| $f_{ACNT}$ | Maximum internal array clock frequency | *(5)* | 151.5 | | 125.0 | | MHz |
| $f_{MAX}$ | Maximum clock frequency | *(6)* | 200 | | 166.7 | | MHz |

**Table 17. MAX 7000 & MAX 7000E Internal Timing Parameters** *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade -6 | | Speed Grade -7 | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $t_{IN}$ | Input pad and buffer delay | | | 0.4 | | 0.5 | ns |
| $t_{IO}$ | I/O input pad and buffer delay | | | 0.4 | | 0.5 | ns |
| $t_{FIN}$ | Fast input delay | *(2)* | | 0.8 | | 1.0 | ns |
| $t_{SEXP}$ | Shared expander delay | | | 3.5 | | 4.0 | ns |
| $t_{PEXP}$ | Parallel expander delay | | | 0.8 | | 0.8 | ns |
| $t_{LAD}$ | Logic array delay | | | 2.0 | | 3.0 | ns |
| $t_{LAC}$ | Logic control array delay | | | 2.0 | | 3.0 | ns |
| $t_{IOE}$ | Internal output enable delay | *(2)* | | | | 2.0 | ns |
| $t_{OD1}$ | Output buffer and pad delay<br>Slow slew rate = off, $V_{CCIO}$ = 5.0 V | C1 = 35 pF | | 2.0 | | 2.0 | ns |
| $t_{OD2}$ | Output buffer and pad delay<br>Slow slew rate = off, $V_{CCIO}$ = 3.3 V | C1 = 35 pF *(7)* | | 2.5 | | 2.5 | ns |
| $t_{OD3}$ | Output buffer and pad delay<br>Slow slew rate = on,<br>$V_{CCIO}$ = 5.0 V or 3.3 V | C1 = 35 pF *(2)* | | 7.0 | | 7.0 | ns |
| $t_{ZX1}$ | Output buffer enable delay<br>Slow slew rate = off, $V_{CCIO}$ = 5.0 V | C1 = 35 pF | | 4.0 | | 4.0 | ns |
| $t_{ZX2}$ | Output buffer enable delay<br>Slow slew rate = off, $V_{CCIO}$ = 3.3 V | C1 = 35 pF *(7)* | | 4.5 | | 4.5 | ns |
| $t_{ZX3}$ | Output buffer enable delay<br>Slow slew rate = on<br>$V_{CCIO}$ = 5.0 V or 3.3 V | C1 = 35 pF *(2)* | | 9.0 | | 9.0 | ns |
| $t_{XZ}$ | Output buffer disable delay | C1 = 5 pF | | 4.0 | | 4.0 | ns |
| $t_{SU}$ | Register setup time | | 3.0 | | 3.0 | | ns |
| $t_{H}$ | Register hold time | | 1.5 | | 2.0 | | ns |
| $t_{FSU}$ | Register setup time of fast input | *(2)* | 2.5 | | 3.0 | | ns |
| $t_{FH}$ | Register hold time of fast input | *(2)* | 0.5 | | 0.5 | | ns |
| $t_{RD}$ | Register delay | | | 0.8 | | 1.0 | ns |
| $t_{COMB}$ | Combinatorial delay | | | 0.8 | | 1.0 | ns |
| $t_{IC}$ | Array clock delay | | | 2.5 | | 3.0 | ns |
| $t_{EN}$ | Register enable time | | | 2.0 | | 3.0 | ns |
| $t_{GLOB}$ | Global control delay | | | 0.8 | | 1.0 | ns |
| $t_{PRE}$ | Register preset time | | | 2.0 | | 2.0 | ns |
| $t_{CLR}$ | Register clear time | | | 2.0 | | 2.0 | ns |
| $t_{PIA}$ | PIA delay | | | 0.8 | | 1.0 | ns |
| $t_{LPA}$ | Low-power adder | *(8)* | | 10.0 | | 10.0 | ns |

*Table 18. MAX 7000 & MAX 7000E External Timing Parameters* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | MAX 7000E (-10P) | | MAX 7000 (-10) MAX 7000E (-10) | | |
| | | | Min | Max | Min | Max | |
| $t_{PD1}$ | Input to non-registered output | C1 = 35 pF | | 10.0 | | 10.0 | ns |
| $t_{PD2}$ | I/O input to non-registered output | C1 = 35 pF | | 10.0 | | 10.0 | ns |
| $t_{SU}$ | Global clock setup time | | 7.0 | | 8.0 | | ns |
| $t_{H}$ | Global clock hold time | | 0.0 | | 0.0 | | ns |
| $t_{FSU}$ | Global clock setup time of fast input | *(2)* | 3.0 | | 3.0 | | ns |
| $t_{FH}$ | Global clock hold time of fast input | *(2)* | 0.5 | | 0.5 | | ns |
| $t_{CO1}$ | Global clock to output delay | C1 = 35 pF | | 5.0 | | 5 | ns |
| $t_{CH}$ | Global clock high time | | 4.0 | | 4.0 | | ns |
| $t_{CL}$ | Global clock low time | | 4.0 | | 4.0 | | ns |
| $t_{ASU}$ | Array clock setup time | | 2.0 | | 3.0 | | ns |
| $t_{AH}$ | Array clock hold time | | 3.0 | | 3.0 | | ns |
| $t_{ACO1}$ | Array clock to output delay | C1 = 35 pF | | 10.0 | | 10.0 | ns |
| $t_{ACH}$ | Array clock high time | | 4.0 | | 4.0 | | ns |
| $t_{ACL}$ | Array clock low time | | 4.0 | | 4.0 | | ns |
| $t_{CPPW}$ | Minimum pulse width for clear and preset | *(3)* | 4.0 | | 4.0 | | ns |
| $t_{ODH}$ | Output data hold time after clock | C1 = 35 pF *(4)* | 1.0 | | 1.0 | | ns |
| $t_{CNT}$ | Minimum global clock period | | | 10.0 | | 10.0 | ns |
| $f_{CNT}$ | Maximum internal global clock frequency | *(5)* | 100.0 | | 100.0 | | MHz |
| $t_{ACNT}$ | Minimum array clock period | | | 10.0 | | 10.0 | ns |
| $f_{ACNT}$ | Maximum internal array clock frequency | *(5)* | 100.0 | | 100.0 | | MHz |
| $f_{MAX}$ | Maximum clock frequency | *(6)* | 125.0 | | 125.0 | | MHz |

*Table 19. MAX 7000 & MAX 7000E Internal Timing Parameters* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | MAX 7000E (-10P) | | MAX 7000 (-10) MAX 7000E (-10) | | |
| | | | Min | Max | Min | Max | |
| $t_{IN}$ | Input pad and buffer delay | | | 0.5 | | 1.0 | ns |
| $t_{IO}$ | I/O input pad and buffer delay | | | 0.5 | | 1.0 | ns |
| $t_{FIN}$ | Fast input delay | *(2)* | | 1.0 | | 1.0 | ns |
| $t_{SEXP}$ | Shared expander delay | | | 5.0 | | 5.0 | ns |
| $t_{PEXP}$ | Parallel expander delay | | | 0.8 | | 0.8 | ns |
| $t_{LAD}$ | Logic array delay | | | 5.0 | | 5.0 | ns |
| $t_{LAC}$ | Logic control array delay | | | 5.0 | | 5.0 | ns |
| $t_{IOE}$ | Internal output enable delay | *(2)* | | 2.0 | | 2.0 | ns |
| $t_{OD1}$ | Output buffer and pad delay<br>Slow slew rate = off<br>$V_{CCIO}$ = 5.0 V | C1 = 35 pF | | 1.5 | | 2.0 | ns |
| $t_{OD2}$ | Output buffer and pad delay<br>Slow slew rate = off<br>$V_{CCIO}$ = 3.3 V | C1 = 35 pF *(7)* | | 2.0 | | 2.5 | ns |
| $t_{OD3}$ | Output buffer and pad delay<br>Slow slew rate = on<br>$V_{CCIO}$ = 5.0 V or 3.3 V | C1 = 35 pF *(2)* | | 5.5 | | 6.0 | ns |
| $t_{ZX1}$ | Output buffer enable delay<br>Slow slew rate = off<br>$V_{CCIO}$ = 5.0 V | C1 = 35 pF | | 5.0 | | 5.0 | ns |
| $t_{ZX2}$ | Output buffer enable delay<br>Slow slew rate = off<br>$V_{CCIO}$ = 3.3 V | C1 = 35 pF *(7)* | | 5.5 | | 5.5 | ns |
| $t_{ZX3}$ | Output buffer enable delay<br>Slow slew rate = on<br>$V_{CCIO}$ = 5.0 V or 3.3 V | C1 = 35 pF *(2)* | | 9.0 | | 9.0 | ns |
| $t_{XZ}$ | Output buffer disable delay | C1 = 5 pF | | 5.0 | | 5.0 | ns |
| $t_{SU}$ | Register setup time | | 2.0 | | 3.0 | | ns |
| $t_{H}$ | Register hold time | | 3.0 | | 3.0 | | ns |
| $t_{FSU}$ | Register setup time of fast input | *(2)* | 3.0 | | 3.0 | | ns |
| $t_{FH}$ | Register hold time of fast input | *(2)* | 0.5 | | 0.5 | | ns |
| $t_{RD}$ | Register delay | | | 2.0 | | 1.0 | ns |
| $t_{COMB}$ | Combinatorial delay | | | 2.0 | | 1.0 | ns |
| $t_{IC}$ | Array clock delay | | | 5.0 | | 5.0 | ns |
| $t_{EN}$ | Register enable time | | | 5.0 | | 5.0 | ns |
| $t_{GLOB}$ | Global control delay | | | 1.0 | | 1.0 | ns |
| $t_{PRE}$ | Register preset time | | | 3.0 | | 3.0 | ns |
| $t_{CLR}$ | Register clear time | | | 3.0 | | 3.0 | ns |
| $t_{PIA}$ | PIA delay | | | 1.0 | | 1.0 | ns |
| $t_{LPA}$ | Low-power adder | *(8)* | | 11.0 | | 11.0 | ns |

*Table 20. MAX 7000 & MAX 7000E External Timing Parameters* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | MAX 7000E (-12P) | | MAX 7000 (-12) MAX 7000E (-12) | | |
| | | | Min | Max | Min | Max | |
| $t_{PD1}$ | Input to non-registered output | C1 = 35 pF | | 12.0 | | 12.0 | ns |
| $t_{PD2}$ | I/O input to non-registered output | C1 = 35 pF | | 12.0 | | 12.0 | ns |
| $t_{SU}$ | Global clock setup time | | 7.0 | | 10.0 | | ns |
| $t_{H}$ | Global clock hold time | | 0.0 | | 0.0 | | ns |
| $t_{FSU}$ | Global clock setup time of fast input | *(2)* | 3.0 | | 3.0 | | ns |
| $t_{FH}$ | Global clock hold time of fast input | *(2)* | 0.0 | | 0.0 | | ns |
| $t_{CO1}$ | Global clock to output delay | C1 = 35 pF | | 6.0 | | 6.0 | ns |
| $t_{CH}$ | Global clock high time | | 4.0 | | 4.0 | | ns |
| $t_{CL}$ | Global clock low time | | 4.0 | | 4.0 | | ns |
| $t_{ASU}$ | Array clock setup time | | 3.0 | | 4.0 | | ns |
| $t_{AH}$ | Array clock hold time | | 4.0 | | 4.0 | | ns |
| $t_{ACO1}$ | Array clock to output delay | C1 = 35 pF | | 12.0 | | 12.0 | ns |
| $t_{ACH}$ | Array clock high time | | 5.0 | | 5.0 | | ns |
| $t_{ACL}$ | Array clock low time | | 5.0 | | 5.0 | | ns |
| $t_{CPPW}$ | Minimum pulse width for clear and preset | *(3)* | 5.0 | | 5.0 | | ns |
| $t_{ODH}$ | Output data hold time after clock | C1 = 35 pF *(4)* | 1.0 | | 1.0 | | ns |
| $t_{CNT}$ | Minimum global clock period | | | 11.0 | | 11.0 | ns |
| $f_{CNT}$ | Maximum internal global clock frequency | *(5)* | 90.9 | | 90.9 | | MHz |
| $t_{ACNT}$ | Minimum array clock period | | | 11.0 | | 11.0 | ns |
| $f_{ACNT}$ | Maximum internal array clock frequency | *(5)* | 90.9 | | 90.9 | | MHz |
| $f_{MAX}$ | Maximum clock frequency | *(6)* | 125.0 | | 125.0 | | MHz |

*Table 21. MAX 7000 & MAX 7000E Internal Timing Parameters* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | MAX 7000E (-12P) | | MAX 7000 (-12) MAX 7000E (-12) | | |
| | | | Min | Max | Min | Max | |
| $t_{IN}$ | Input pad and buffer delay | | | 1.0 | | 2.0 | ns |
| $t_{IO}$ | I/O input pad and buffer delay | | | 1.0 | | 2.0 | ns |
| $t_{FIN}$ | Fast input delay | *(2)* | | 1.0 | | 1.0 | ns |
| $t_{SEXP}$ | Shared expander delay | | | 7.0 | | 7.0 | ns |
| $t_{PEXP}$ | Parallel expander delay | | | 1.0 | | 1.0 | ns |
| $t_{LAD}$ | Logic array delay | | | 7.0 | | 5.0 | ns |
| $t_{LAC}$ | Logic control array delay | | | 5.0 | | 5.0 | ns |
| $t_{IOE}$ | Internal output enable delay | *(2)* | | 2.0 | | 2.0 | ns |
| $t_{OD1}$ | Output buffer and pad delay<br>Slow slew rate = off<br>$V_{CCIO}$ = 5.0 V | C1 = 35 pF | | 1.0 | | 3.0 | ns |
| $t_{OD2}$ | Output buffer and pad delay<br>Slow slew rate = off<br>$V_{CCIO}$ = 3.3 V | C1 = 35 pF *(7)* | | 2.0 | | 4.0 | ns |
| $t_{OD3}$ | Output buffer and pad delay<br>Slow slew rate = on<br>$V_{CCIO}$ = 5.0 V or 3.3 V | C1 = 35 pF *(2)* | | 5.0 | | 7.0 | ns |
| $t_{ZX1}$ | Output buffer enable delay<br>Slow slew rate = off<br>$V_{CCIO}$ = 5.0 V | C1 = 35 pF | | 6.0 | | 6.0 | ns |
| $t_{ZX2}$ | Output buffer enable delay<br>Slow slew rate = off<br>$V_{CCIO}$ = 3.3 V | C1 = 35 pF *(7)* | | 7.0 | | 7.0 | ns |
| $t_{ZX3}$ | Output buffer enable delay<br>Slow slew rate = on<br>$V_{CCIO}$ = 5.0 V or 3.3 V | C1 = 35 pF *(2)* | | 10.0 | | 10.0 | ns |
| $t_{XZ}$ | Output buffer disable delay | C1 = 5 pF | | 6.0 | | 6.0 | ns |
| $t_{SU}$ | Register setup time | | 1.0 | | 4.0 | | ns |
| $t_{H}$ | Register hold time | | 6.0 | | 4.0 | | ns |
| $t_{FSU}$ | Register setup time of fast input | *(2)* | 4.0 | | 2.0 | | ns |
| $t_{FH}$ | Register hold time of fast input | *(2)* | 0.0 | | 2.0 | | ns |
| $t_{RD}$ | Register delay | | | 2.0 | | 1.0 | ns |
| $t_{COMB}$ | Combinatorial delay | | | 2.0 | | 1.0 | ns |
| $t_{IC}$ | Array clock delay | | | 5.0 | | 5.0 | ns |
| $t_{EN}$ | Register enable time | | | 7.0 | | 5.0 | ns |
| $t_{GLOB}$ | Global control delay | | | 2.0 | | 0.0 | ns |
| $t_{PRE}$ | Register preset time | | | 4.0 | | 3.0 | ns |
| $t_{CLR}$ | Register clear time | | | 4.0 | | 3.0 | ns |
| $t_{PIA}$ | PIA delay | | | 1.0 | | 1.0 | ns |
| $t_{LPA}$ | Low-power adder | *(8)* | | 12.0 | | 12.0 | ns |

*Table 22. MAX 7000 & MAX 7000E External Timing Parameters* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | -15 | | -15T | | -20 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{PD1}$ | Input to non-registered output | C1 = 35 pF | | 15.0 | | 15.0 | | 20.0 | ns |
| $t_{PD2}$ | I/O input to non-registered output | C1 = 35 pF | | 15.0 | | 15.0 | | 20.0 | ns |
| $t_{SU}$ | Global clock setup time | | 11.0 | | 11.0 | | 12.0 | | ns |
| $t_{H}$ | Global clock hold time | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{FSU}$ | Global clock setup time of fast input | *(2)* | 3.0 | | – | | 5.0 | | ns |
| $t_{FH}$ | Global clock hold time of fast input | *(2)* | 0.0 | | – | | 0.0 | | ns |
| $t_{CO1}$ | Global clock to output delay | C1 = 35 pF | | 8.0 | | 8.0 | | 12.0 | ns |
| $t_{CH}$ | Global clock high time | | 5.0 | | 6.0 | | 6.0 | | ns |
| $t_{CL}$ | Global clock low time | | 5.0 | | 6.0 | | 6.0 | | ns |
| $t_{ASU}$ | Array clock setup time | | 4.0 | | 4.0 | | 5.0 | | ns |
| $t_{AH}$ | Array clock hold time | | 4.0 | | 4.0 | | 5.0 | | ns |
| $t_{ACO1}$ | Array clock to output delay | C1 = 35 pF | | 15.0 | | 15.0 | | 20.0 | ns |
| $t_{ACH}$ | Array clock high time | | 6.0 | | 6.5 | | 8.0 | | ns |
| $t_{ACL}$ | Array clock low time | | 6.0 | | 6.5 | | 8.0 | | ns |
| $t_{CPPW}$ | Minimum pulse width for clear and preset | *(3)* | 6.0 | | 6.5 | | 8.0 | | ns |
| $t_{ODH}$ | Output data hold time after clock | C1 = 35 pF *(4)* | 1.0 | | 1.0 | | 1.0 | | ns |
| $t_{CNT}$ | Minimum global clock period | | | 13.0 | | 13.0 | | 16.0 | ns |
| $f_{CNT}$ | Maximum internal global clock frequency | *(5)* | 76.9 | | 76.9 | | 62.5 | | MHz |
| $t_{ACNT}$ | Minimum array clock period | | | 13.0 | | 13.0 | | 16.0 | ns |
| $f_{ACNT}$ | Maximum internal array clock frequency | *(5)* | 76.9 | | 76.9 | | 62.5 | | MHz |
| $f_{MAX}$ | Maximum clock frequency | *(6)* | 100 | | 83.3 | | 83.3 | | MHz |

*Table 23. MAX 7000 & MAX 7000E Internal Timing Parameters* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | -15 | | -15T | | -20 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{IN}$ | Input pad and buffer delay | | | 2.0 | | 2.0 | | 3.0 | ns |
| $t_{IO}$ | I/O input pad and buffer delay | | | 2.0 | | 2.0 | | 3.0 | ns |
| $t_{FIN}$ | Fast input delay | *(2)* | | 2.0 | | – | | 4.0 | ns |
| $t_{SEXP}$ | Shared expander delay | | | 8.0 | | 10.0 | | 9.0 | ns |
| $t_{PEXP}$ | Parallel expander delay | | | 1.0 | | 1.0 | | 2.0 | ns |
| $t_{LAD}$ | Logic array delay | | | 6.0 | | 6.0 | | 8.0 | ns |
| $t_{LAC}$ | Logic control array delay | | | 6.0 | | 6.0 | | 8.0 | ns |
| $t_{IOE}$ | Internal output enable delay | *(2)* | | 3.0 | | – | | 4.0 | ns |
| $t_{OD1}$ | Output buffer and pad delay<br>Slow slew rate = off<br>$V_{CCIO}$ = 5.0 V | C1 = 35 pF | | 4.0 | | 4.0 | | 5.0 | ns |
| $t_{OD2}$ | Output buffer and pad delay<br>Slow slew rate = off<br>$V_{CCIO}$ = 3.3 V | C1 = 35 pF *(7)* | | 5.0 | | – | | 6.0 | ns |
| $t_{OD3}$ | Output buffer and pad delay<br>Slow slew rate = on<br>$V_{CCIO}$ = 5.0 V or 3.3 V | C1 = 35 pF *(2)* | | 8.0 | | – | | 9.0 | ns |
| $t_{ZX1}$ | Output buffer enable delay<br>Slow slew rate = off<br>$V_{CCIO}$ = 5.0 V | C1 = 35 pF | | 6.0 | | 6.0 | | 10.0 | ns |
| $t_{ZX2}$ | Output buffer enable delay<br>Slow slew rate = off<br>$V_{CCIO}$ = 3.3 V | C1 = 35 pF *(7)* | | 7.0 | | – | | 11.0 | ns |
| $t_{ZX3}$ | Output buffer enable delay<br>Slow slew rate = on<br>$V_{CCIO}$ = 5.0 V or 3.3 V | C1 = 35 pF *(2)* | | 10.0 | | – | | 14.0 | ns |
| $t_{XZ}$ | Output buffer disable delay | C1 = 5 pF | | 6.0 | | 6.0 | | 10.0 | ns |
| $t_{SU}$ | Register setup time | | 4.0 | | 4.0 | | 4.0 | | ns |
| $t_{H}$ | Register hold time | | 4.0 | | 4.0 | | 5.0 | | ns |
| $t_{FSU}$ | Register setup time of fast input | *(2)* | 2.0 | | – | | 4.0 | | ns |
| $t_{FH}$ | Register hold time of fast input | *(2)* | 2.0 | | – | | 3.0 | | ns |
| $t_{RD}$ | Register delay | | | 1.0 | | 1.0 | | 1.0 | ns |
| $t_{COMB}$ | Combinatorial delay | | | 1.0 | | 1.0 | | 1.0 | ns |
| $t_{IC}$ | Array clock delay | | | 6.0 | | 6.0 | | 8.0 | ns |
| $t_{EN}$ | Register enable time | | | 6.0 | | 6.0 | | 8.0 | ns |
| $t_{GLOB}$ | Global control delay | | | 1.0 | | 1.0 | | 3.0 | ns |
| $t_{PRE}$ | Register preset time | | | 4.0 | | 4.0 | | 4.0 | ns |
| $t_{CLR}$ | Register clear time | | | 4.0 | | 4.0 | | 4.0 | ns |
| $t_{PIA}$ | PIA delay | | | 2.0 | | 2.0 | | 3.0 | ns |
| $t_{LPA}$ | Low-power adder | *(8)* | | 13.0 | | 15.0 | | 15.0 | ns |

*Notes to tables:*

(1) These values are specified under the recommended operating conditions shown in Table 11. See Figure 13 for more information on switching waveforms.
(2) This parameter applies to MAX 7000E devices only.
(3) This minimum pulse width for preset and clear applies for both global clear and array controls. The $t_{LPA}$ parameter must be added to this minimum width if the clear or reset signal incorporates the $t_{LAD}$ parameter into the signal path.
(4) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
(5) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
(6) The $\mathbf{f_{MAX}}$ values represent the highest frequency for pipelined data.
(7) Operating conditions: $V_{CCIO}$ = 3.3 V ± 10% for commercial and industrial use.
(8) The $t_{LPA}$ parameter must be added to the $t_{LAD}$, $t_{LAC}$, $t_{IC}$, $t_{EN}$, $t_{SEXP}$, $\mathbf{t_{ACL}}$, and $\mathbf{t_{CPPW}}$ parameters for macrocells running in the low-power mode.

Tables 24 and 25 show the EPM7032S AC operating conditions.

***Table 24. EPM7032S External Timing Parameters (Part 1 of 2)*** *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | -5 | | -6 | | -7 | | -10 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $\mathbf{t_{PD1}}$ | Input to non-registered output | C1 = 35 pF | | 5.0 | | 6.0 | | 7.5 | | 10.0 | ns |
| $\mathbf{t_{PD2}}$ | I/O input to non-registered output | C1 = 35 pF | | 5.0 | | 6.0 | | 7.5 | | 10.0 | ns |
| $\mathbf{t_{SU}}$ | Global clock setup time | | 2.9 | | 4.0 | | 5.0 | | 7.0 | | ns |
| $\mathbf{t_{H}}$ | Global clock hold time | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $\mathbf{t_{FSU}}$ | Global clock setup time of fast input | | 2.5 | | 2.5 | | 2.5 | | 3.0 | | ns |
| $\mathbf{t_{FH}}$ | Global clock hold time of fast input | | 0.0 | | 0.0 | | 0.0 | | 0.5 | | ns |
| $\mathbf{t_{CO1}}$ | Global clock to output delay | C1 = 35 pF | | 3.2 | | 3.5 | | 4.3 | | 5.0 | ns |
| $\mathbf{t_{CH}}$ | Global clock high time | | 2.0 | | 2.5 | | 3.0 | | 4.0 | | ns |
| $\mathbf{t_{CL}}$ | Global clock low time | | 2.0 | | 2.5 | | 3.0 | | 4.0 | | ns |
| $\mathbf{t_{ASU}}$ | Array clock setup time | | 0.7 | | 0.9 | | 1.1 | | 2.0 | | ns |
| $\mathbf{t_{AH}}$ | Array clock hold time | | 1.8 | | 2.1 | | 2.7 | | 3.0 | | ns |
| $\mathbf{t_{ACO1}}$ | Array clock to output delay | C1 = 35 pF | | 5.4 | | 6.6 | | 8.2 | | 10.0 | ns |
| $\mathbf{t_{ACH}}$ | Array clock high time | | 2.5 | | 2.5 | | 3.0 | | 4.0 | | ns |
| $\mathbf{t_{ACL}}$ | Array clock low time | | 2.5 | | 2.5 | | 3.0 | | 4.0 | | ns |
| $\mathbf{t_{CPPW}}$ | Minimum pulse width for clear and preset | *(2)* | 2.5 | | 2.5 | | 3.0 | | 4.0 | | ns |
| $\mathbf{t_{ODH}}$ | Output data hold time after clock | C1 = 35 pF *(3)* | 1.0 | | 1.0 | | 1.0 | | 1.0 | | ns |
| $\mathbf{t_{CNT}}$ | Minimum global clock period | | | 5.7 | | 7.0 | | 8.6 | | 10.0 | ns |
| $\mathbf{f_{CNT}}$ | Maximum internal global clock frequency | *(4)* | 175.4 | | 142.9 | | 116.3 | | 100.0 | | MHz |
| $\mathbf{t_{ACNT}}$ | Minimum array clock period | | | 5.7 | | 7.0 | | 8.6 | | 10.0 | ns |

*Table 24. EPM7032S External Timing Parameters (Part 2 of 2)* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | -5 | | -6 | | -7 | | -10 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $f_{ACNT}$ | Maximum internal array clock frequency | *(4)* | 175.4 | | 142.9 | | 116.3 | | 100.0 | | MHz |
| $f_{MAX}$ | Maximum clock frequency | *(5)* | 250.0 | | 200.0 | | 166.7 | | 125.0 | | MHz |

*Table 25. EPM7032S Internal Timing Parameters* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | -5 | | -6 | | -7 | | -10 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{IN}$ | Input pad and buffer delay | | | 0.2 | | 0.2 | | 0.3 | | 0.5 | ns |
| $t_{IO}$ | I/O input pad and buffer delay | | | 0.2 | | 0.2 | | 0.3 | | 0.5 | ns |
| $t_{FIN}$ | Fast input delay | | | 2.2 | | 2.1 | | 2.5 | | 1.0 | ns |
| $t_{SEXP}$ | Shared expander delay | | | 3.1 | | 3.8 | | 4.6 | | 5.0 | ns |
| $t_{PEXP}$ | Parallel expander delay | | | 0.9 | | 1.1 | | 1.4 | | 0.8 | ns |
| $t_{LAD}$ | Logic array delay | | | 2.6 | | 3.3 | | 4.0 | | 5.0 | ns |
| $t_{LAC}$ | Logic control array delay | | | 2.5 | | 3.3 | | 4.0 | | 5.0 | ns |
| $t_{IOE}$ | Internal output enable delay | | | 0.7 | | 0.8 | | 1.0 | | 2.0 | ns |
| $t_{OD1}$ | Output buffer and pad delay | C1 = 35 pF | | 0.2 | | 0.3 | | 0.4 | | 1.5 | ns |
| $t_{OD2}$ | Output buffer and pad delay | C1 = 35 pF *(6)* | | 0.7 | | 0.8 | | 0.9 | | 2.0 | ns |
| $t_{OD3}$ | Output buffer and pad delay | C1 = 35 pF | | 5.2 | | 5.3 | | 5.4 | | 5.5 | ns |
| $t_{ZX1}$ | Output buffer enable delay | C1 = 35 pF | | 4.0 | | 4.0 | | 4.0 | | 5.0 | ns |
| $t_{ZX2}$ | Output buffer enable delay | C1 = 35 pF *(6)* | | 4.5 | | 4.5 | | 4.5 | | 5.5 | ns |
| $t_{ZX3}$ | Output buffer enable delay | C1 = 35 pF | | 9.0 | | 9.0 | | 9.0 | | 9.0 | ns |
| $t_{XZ}$ | Output buffer disable delay | C1 = 5 pF | | 4.0 | | 4.0 | | 4.0 | | 5.0 | ns |
| $t_{SU}$ | Register setup time | | 0.8 | | 1.0 | | 1.3 | | 2.0 | | ns |
| $t_{H}$ | Register hold time | | 1.7 | | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{FSU}$ | Register setup time of fast input | | 1.9 | | 1.8 | | 1.7 | | 3.0 | | ns |
| $t_{FH}$ | Register hold time of fast input | | 0.6 | | 0.7 | | 0.8 | | 0.5 | | ns |
| $t_{RD}$ | Register delay | | | 1.2 | | 1.6 | | 1.9 | | 2.0 | ns |
| $t_{COMB}$ | Combinatorial delay | | | 0.9 | | 1.1 | | 1.4 | | 2.0 | ns |
| $t_{IC}$ | Array clock delay | | | 2.7 | | 3.4 | | 4.2 | | 5.0 | ns |
| $t_{EN}$ | Register enable time | | | 2.6 | | 3.3 | | 4.0 | | 5.0 | ns |
| $t_{GLOB}$ | Global control delay | | | 1.6 | | 1.4 | | 1.7 | | 1.0 | ns |
| $t_{PRE}$ | Register preset time | | | 2.0 | | 2.4 | | 3.0 | | 3.0 | ns |

**Table 25. EPM7032S Internal Timing Parameters** *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | -5 | | -6 | | -7 | | -10 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{CLR}$ | Register clear time | | | 2.0 | | 2.4 | | 3.0 | | 3.0 | ns |
| $t_{PIA}$ | PIA delay | *(7)* | | 1.1 | | 1.1 | | 1.4 | | 1.0 | ns |
| $t_{LPA}$ | Low-power adder | *(8)* | | 12.0 | | 10.0 | | 10.0 | | 11.0 | ns |

*Notes to tables:*

(1) These values are specified under the recommended operating conditions shown in Table 11. See Figure 13 for more information on switching waveforms.
(2) This minimum pulse width for preset and clear applies for both global clear and array controls. The $t_{LPA}$ parameter must be added to this minimum width if the clear or reset signal incorporates the $t_{LAD}$ parameter into the signal path.
(3) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
(4) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
(5) The $\mathbf{f_{MAX}}$ values represent the highest frequency for pipelined data.
(6) Operating conditions: $V_{CCIO}$ = 3.3 V ± 10% for commercial and industrial use.
(7) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
(8) The $t_{LPA}$ parameter must be added to the $t_{LAD}$, $t_{LAC}$, $t_{IC}$, $t_{EN}$, $t_{SEXP}$, $\mathbf{t_{ACL}}$, and $\mathbf{t_{CPPW}}$ parameters for macrocells running in the low-power mode.

Tables 26 and 27 show the EPM7064S AC operating conditions.

**Table 26. EPM7064S External Timing Parameters (Part 1 of 2)** *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | -5 | | -6 | | -7 | | -10 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $\mathbf{t_{PD1}}$ | Input to non-registered output | C1 = 35 pF | | 5.0 | | 6.0 | | 7.5 | | 10.0 | ns |
| $\mathbf{t_{PD2}}$ | I/O input to non-registered output | C1 = 35 pF | | 5.0 | | 6.0 | | 7.5 | | 10.0 | ns |
| $\mathbf{t_{SU}}$ | Global clock setup time | | 2.9 | | 3.6 | | 6.0 | | 7.0 | | ns |
| $\mathbf{t_{H}}$ | Global clock hold time | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $\mathbf{t_{FSU}}$ | Global clock setup time of fast input | | 2.5 | | 2.5 | | 3.0 | | 3.0 | | ns |
| $\mathbf{t_{FH}}$ | Global clock hold time of fast input | | 0.0 | | 0.0 | | 0.5 | | 0.5 | | ns |
| $\mathbf{t_{CO1}}$ | Global clock to output delay | C1 = 35 pF | | 3.2 | | 4.0 | | 4.5 | | 5.0 | ns |
| $\mathbf{t_{CH}}$ | Global clock high time | | 2.0 | | 2.5 | | 3.0 | | 4.0 | | ns |
| $\mathbf{t_{CL}}$ | Global clock low time | | 2.0 | | 2.5 | | 3.0 | | 4.0 | | ns |
| $\mathbf{t_{ASU}}$ | Array clock setup time | | 0.7 | | 0.9 | | 3.0 | | 2.0 | | ns |

*Table 26. EPM7064S External Timing Parameters (Part 2 of 2)* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | -5 | | -6 | | -7 | | -10 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{AH}$ | Array clock hold time | | 1.8 | | 2.1 | | 2.0 | | 3.0 | | ns |
| $t_{ACO1}$ | Array clock to output delay | C1 = 35 pF | | 5.4 | | 6.7 | | 7.5 | | 10.0 | ns |
| $t_{ACH}$ | Array clock high time | | 2.5 | | 2.5 | | 3.0 | | 4.0 | | ns |
| $t_{ACL}$ | Array clock low time | | 2.5 | | 2.5 | | 3.0 | | 4.0 | | ns |
| $t_{CPPW}$ | Minimum pulse width for clear and preset | *(2)* | 2.5 | | 2.5 | | 3.0 | | 4.0 | | ns |
| $t_{ODH}$ | Output data hold time after clock | C1 = 35 pF *(3)* | 1.0 | | 1.0 | | 1.0 | | 1.0 | | ns |
| $t_{CNT}$ | Minimum global clock period | | | 5.7 | | 7.1 | | 8.0 | | 10.0 | ns |
| $f_{CNT}$ | Maximum internal global clock frequency | *(4)* | 175.4 | | 140.8 | | 125.0 | | 100.0 | | MHz |
| $t_{ACNT}$ | Minimum array clock period | | | 5.7 | | 7.1 | | 8.0 | | 10.0 | ns |
| $f_{ACNT}$ | Maximum internal array clock frequency | *(4)* | 175.4 | | 140.8 | | 125.0 | | 100.0 | | MHz |
| $f_{MAX}$ | Maximum clock frequency | *(5)* | 250.0 | | 200.0 | | 166.7 | | 125.0 | | MHz |

*Table 27. EPM7064S Internal Timing Parameters (Part 1 of 2)* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | -5 | | -6 | | -7 | | -10 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{IN}$ | Input pad and buffer delay | | | 0.2 | | 0.2 | | 0.5 | | 0.5 | ns |
| $t_{IO}$ | I/O input pad and buffer delay | | | 0.2 | | 0.2 | | 0.5 | | 0.5 | ns |
| $t_{FIN}$ | Fast input delay | | | 2.2 | | 2.6 | | 1.0 | | 1.0 | ns |
| $t_{SEXP}$ | Shared expander delay | | | 3.1 | | 3.8 | | 4.0 | | 5.0 | ns |
| $t_{PEXP}$ | Parallel expander delay | | | 0.9 | | 1.1 | | 0.8 | | 0.8 | ns |
| $t_{LAD}$ | Logic array delay | | | 2.6 | | 3.2 | | 3.0 | | 5.0 | ns |
| $t_{LAC}$ | Logic control array delay | | | 2.5 | | 3.2 | | 3.0 | | 5.0 | ns |
| $t_{IOE}$ | Internal output enable delay | | | 0.7 | | 0.8 | | 2.0 | | 2.0 | ns |
| $t_{OD1}$ | Output buffer and pad delay | C1 = 35 pF | | 0.2 | | 0.3 | | 2.0 | | 1.5 | ns |
| $t_{OD2}$ | Output buffer and pad delay | C1 = 35 pF *(6)* | | 0.7 | | 0.8 | | 2.5 | | 2.0 | ns |
| $t_{OD3}$ | Output buffer and pad delay | C1 = 35 pF | | 5.2 | | 5.3 | | 7.0 | | 5.5 | ns |
| $t_{ZX1}$ | Output buffer enable delay | C1 = 35 pF | | 4.0 | | 4.0 | | 4.0 | | 5.0 | ns |
| $t_{ZX2}$ | Output buffer enable delay | C1 = 35 pF *(6)* | | 4.5 | | 4.5 | | 4.5 | | 5.5 | ns |
| $t_{ZX3}$ | Output buffer enable delay | C1 = 35 pF | | 9.0 | | 9.0 | | 9.0 | | 9.0 | ns |
| $t_{XZ}$ | Output buffer disable delay | C1 = 5 pF | | 4.0 | | 4.0 | | 4.0 | | 5.0 | ns |
| $t_{SU}$ | Register setup time | | 0.8 | | 1.0 | | 3.0 | | 2.0 | | ns |

*Table 27. EPM7064S Internal Timing Parameters (Part 2 of 2)* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | -5 | | -6 | | -7 | | -10 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_H$ | Register hold time | | 1.7 | | 2.0 | | 2.0 | | 3.0 | | ns |
| $t_{FSU}$ | Register setup time of fast input | | 1.9 | | 1.8 | | 3.0 | | 3.0 | | ns |
| $t_{FH}$ | Register hold time of fast input | | 0.6 | | 0.7 | | 0.5 | | 0.5 | | ns |
| $t_{RD}$ | Register delay | | | 1.2 | | 1.6 | | 1.0 | | 2.0 | ns |
| $t_{COMB}$ | Combinatorial delay | | | 0.9 | | 1.0 | | 1.0 | | 2.0 | ns |
| $t_{IC}$ | Array clock delay | | | 2.7 | | 3.3 | | 3.0 | | 5.0 | ns |
| $t_{EN}$ | Register enable time | | | 2.6 | | 3.2 | | 3.0 | | 5.0 | ns |
| $t_{GLOB}$ | Global control delay | | | 1.6 | | 1.9 | | 1.0 | | 1.0 | ns |
| $t_{PRE}$ | Register preset time | | | 2.0 | | 2.4 | | 2.0 | | 3.0 | ns |
| $t_{CLR}$ | Register clear time | | | 2.0 | | 2.4 | | 2.0 | | 3.0 | ns |
| $t_{PIA}$ | PIA delay | *(7)* | | 1.1 | | 1.3 | | 1.0 | | 1.0 | ns |
| $t_{LPA}$ | Low-power adder | *(8)* | | 12.0 | | 11.0 | | 10.0 | | 11.0 | ns |

*Notes to tables:*

(1) These values are specified under the recommended operating conditions shown in Table 11. See Figure 13 for more information on switching waveforms.

(2) This minimum pulse width for preset and clear applies for both global clear and array controls. The $t_{LPA}$ parameter must be added to this minimum width if the clear or reset signal incorporates the $t_{LAD}$ parameter into the signal path.

(3) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.

(4) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.

(5) The $\mathbf{f_{MAX}}$ values represent the highest frequency for pipelined data.

(6) Operating conditions: $V_{CCIO}$ = 3.3 V ± 10% for commercial and industrial use.

(7) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.

(8) The $t_{LPA}$ parameter must be added to the $t_{LAD}$, $t_{LAC}$, $t_{IC}$, $t_{EN}$, $t_{SEXP}$, $\mathbf{t_{ACL}}$, and $\mathbf{t_{CPPW}}$ parameters for macrocells running in the low-power mode.

Tables 28 and 29 show the EPM7128S AC operating conditions.

**Table 28. EPM7128S External Timing Parameters** *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | -6 | | -7 | | -10 | | -15 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{PD1}$ | Input to non-registered output | C1 = 35 pF | | 6.0 | | 7.5 | | 10.0 | | 15.0 | ns |
| $t_{PD2}$ | I/O input to non-registered output | C1 = 35 pF | | 6.0 | | 7.5 | | 10.0 | | 15.0 | ns |
| $t_{SU}$ | Global clock setup time | | 3.4 | | 6.0 | | 7.0 | | 11.0 | | ns |
| $t_{H}$ | Global clock hold time | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{FSU}$ | Global clock setup time of fast input | | 2.5 | | 3.0 | | 3.0 | | 3.0 | | ns |
| $t_{FH}$ | Global clock hold time of fast input | | 0.0 | | 0.5 | | 0.5 | | 0.0 | | ns |
| $t_{CO1}$ | Global clock to output delay | C1 = 35 pF | | 4.0 | | 4.5 | | 5.0 | | 8.0 | ns |
| $t_{CH}$ | Global clock high time | | 3.0 | | 3.0 | | 4.0 | | 5.0 | | ns |
| $t_{CL}$ | Global clock low time | | 3.0 | | 3.0 | | 4.0 | | 5.0 | | ns |
| $t_{ASU}$ | Array clock setup time | | 0.9 | | 3.0 | | 2.0 | | 4.0 | | ns |
| $t_{AH}$ | Array clock hold time | | 1.8 | | 2.0 | | 5.0 | | 4.0 | | ns |
| $t_{ACO1}$ | Array clock to output delay | C1 = 35 pF | | 6.5 | | 7.5 | | 10.0 | | 15.0 | ns |
| $t_{ACH}$ | Array clock high time | | 3.0 | | 3.0 | | 4.0 | | 6.0 | | ns |
| $t_{ACL}$ | Array clock low time | | 3.0 | | 3.0 | | 4.0 | | 6.0 | | ns |
| $t_{CPPW}$ | Minimum pulse width for clear and preset | *(2)* | 3.0 | | 3.0 | | 4.0 | | 6.0 | | ns |
| $t_{ODH}$ | Output data hold time after clock | C1 = 35 pF *(3)* | 1.0 | | 1.0 | | 1.0 | | 1.0 | | ns |
| $t_{CNT}$ | Minimum global clock period | | | 6.8 | | 8.0 | | 10.0 | | 13.0 | ns |
| $f_{CNT}$ | Maximum internal global clock frequency | *(4)* | 147.1 | | 125.0 | | 100.0 | | 76.9 | | MHz |
| $t_{ACNT}$ | Minimum array clock period | | | 6.8 | | 8.0 | | 10.0 | | 13.0 | ns |
| $f_{ACNT}$ | Maximum internal array clock frequency | *(4)* | 147.1 | | 125.0 | | 100.0 | | 76.9 | | MHz |
| $f_{MAX}$ | Maximum clock frequency | *(5)* | 166.7 | | 166.7 | | 125.0 | | 100.0 | | MHz |

*Table 29. EPM7128S Internal Timing Parameters* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | -6 | | -7 | | -10 | | -15 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{IN}$ | Input pad and buffer delay | | | 0.2 | | 0.5 | | 0.5 | | 2.0 | ns |
| $t_{IO}$ | I/O input pad and buffer delay | | | 0.2 | | 0.5 | | 0.5 | | 2.0 | ns |
| $t_{FIN}$ | Fast input delay | | | 2.6 | | 1.0 | | 1.0 | | 2.0 | ns |
| $t_{SEXP}$ | Shared expander delay | | | 3.7 | | 4.0 | | 5.0 | | 8.0 | ns |
| $t_{PEXP}$ | Parallel expander delay | | | 1.1 | | 0.8 | | 0.8 | | 1.0 | ns |
| $t_{LAD}$ | Logic array delay | | | 3.0 | | 3.0 | | 5.0 | | 6.0 | ns |
| $t_{LAC}$ | Logic control array delay | | | 3.0 | | 3.0 | | 5.0 | | 6.0 | ns |
| $t_{IOE}$ | Internal output enable delay | | | 0.7 | | 2.0 | | 2.0 | | 3.0 | ns |
| $t_{OD1}$ | Output buffer and pad delay | C1 = 35 pF | | 0.4 | | 2.0 | | 1.5 | | 4.0 | ns |
| $t_{OD2}$ | Output buffer and pad delay | C1 = 35 pF *(6)* | | 0.9 | | 2.5 | | 2.0 | | 5.0 | ns |
| $t_{OD3}$ | Output buffer and pad delay | C1 = 35 pF | | 5.4 | | 7.0 | | 5.5 | | 8.0 | ns |
| $t_{ZX1}$ | Output buffer enable delay | C1 = 35 pF | | 4.0 | | 4.0 | | 5.0 | | 6.0 | ns |
| $t_{ZX2}$ | Output buffer enable delay | C1 = 35 pF *(6)* | | 4.5 | | 4.5 | | 5.5 | | 7.0 | ns |
| $t_{ZX3}$ | Output buffer enable delay | C1 = 35 pF | | 9.0 | | 9.0 | | 9.0 | | 10.0 | ns |
| $t_{XZ}$ | Output buffer disable delay | C1 = 5 pF | | 4.0 | | 4.0 | | 5.0 | | 6.0 | ns |
| $t_{SU}$ | Register setup time | | 1.0 | | 3.0 | | 2.0 | | 4.0 | | ns |
| $t_{H}$ | Register hold time | | 1.7 | | 2.0 | | 5.0 | | 4.0 | | ns |
| $t_{FSU}$ | Register setup time of fast input | | 1.9 | | 3.0 | | 3.0 | | 2.0 | | ns |
| $t_{FH}$ | Register hold time of fast input | | 0.6 | | 0.5 | | 0.5 | | 1.0 | | ns |
| $t_{RD}$ | Register delay | | | 1.4 | | 1.0 | | 2.0 | | 1.0 | ns |
| $t_{COMB}$ | Combinatorial delay | | | 1.0 | | 1.0 | | 2.0 | | 1.0 | ns |
| $t_{IC}$ | Array clock delay | | | 3.1 | | 3.0 | | 5.0 | | 6.0 | ns |
| $t_{EN}$ | Register enable time | | | 3.0 | | 3.0 | | 5.0 | | 6.0 | ns |
| $t_{GLOB}$ | Global control delay | | | 2.0 | | 1.0 | | 1.0 | | 1.0 | ns |
| $t_{PRE}$ | Register preset time | | | 2.4 | | 2.0 | | 3.0 | | 4.0 | ns |
| $t_{CLR}$ | Register clear time | | | 2.4 | | 2.0 | | 3.0 | | 4.0 | ns |
| $t_{PIA}$ | PIA delay | *(7)* | | 1.4 | | 1.0 | | 1.0 | | 2.0 | ns |
| $t_{LPA}$ | Low-power adder | *(8)* | | 11.0 | | 10.0 | | 11.0 | | 13.0 | ns |

*Notes to tables:*

(1) These values are specified under the recommended operating conditions shown in Table 11. See Figure 13 for more information on switching waveforms.
(2) This minimum pulse width for preset and clear applies for both global clear and array controls. The $t_{LPA}$ parameter must be added to this minimum width if the clear or reset signal incorporates the $t_{LAD}$ parameter into the signal path.
(3) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
(4) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
(5) The $\mathbf{f_{MAX}}$ values represent the highest frequency for pipelined data.
(6) Operating conditions: $V_{CCIO}$ = 3.3 V ± 10% for commercial and industrial use.
(7) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
(8) The $t_{LPA}$ parameter must be added to the $t_{LAD}$, $t_{LAC}$, $t_{IC}$, $t_{EN}$, $t_{SEXP}$, $\mathbf{t_{ACL}}$, and $\mathbf{t_{CPPW}}$ parameters for macrocells running in the low-power mode.

Tables 30 and 31 show the EPM7160S AC operating conditions.

***Table 30. EPM7160S External Timing Parameters (Part 1 of 2)*** *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | -6 | | -7 | | -10 | | -15 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $\mathbf{t_{PD1}}$ | Input to non-registered output | C1 = 35 pF | | 6.0 | | 7.5 | | 10.0 | | 15.0 | ns |
| $\mathbf{t_{PD2}}$ | I/O input to non-registered output | C1 = 35 pF | | 6.0 | | 7.5 | | 10.0 | | 15.0 | ns |
| $\mathbf{t_{SU}}$ | Global clock setup time | | 3.4 | | 4.2 | | 7.0 | | 11.0 | | ns |
| $\mathbf{t_{H}}$ | Global clock hold time | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $\mathbf{t_{FSU}}$ | Global clock setup time of fast input | | 2.5 | | 3.0 | | 3.0 | | 3.0 | | ns |
| $\mathbf{t_{FH}}$ | Global clock hold time of fast input | | 0.0 | | 0.0 | | 0.5 | | 0.0 | | ns |
| $\mathbf{t_{CO1}}$ | Global clock to output delay | C1 = 35 pF | | 3.9 | | 4.8 | | 5 | | 8 | ns |
| $\mathbf{t_{CH}}$ | Global clock high time | | 3.0 | | 3.0 | | 4.0 | | 5.0 | | ns |
| $\mathbf{t_{CL}}$ | Global clock low time | | 3.0 | | 3.0 | | 4.0 | | 5.0 | | ns |
| $\mathbf{t_{ASU}}$ | Array clock setup time | | 0.9 | | 1.1 | | 2.0 | | 4.0 | | ns |
| $\mathbf{t_{AH}}$ | Array clock hold time | | 1.7 | | 2.1 | | 3.0 | | 4.0 | | ns |
| $\mathbf{t_{ACO1}}$ | Array clock to output delay | C1 = 35 pF | | 6.4 | | 7.9 | | 10.0 | | 15.0 | ns |
| $\mathbf{t_{ACH}}$ | Array clock high time | | 3.0 | | 3.0 | | 4.0 | | 6.0 | | ns |
| $\mathbf{t_{ACL}}$ | Array clock low time | | 3.0 | | 3.0 | | 4.0 | | 6.0 | | ns |
| $\mathbf{t_{CPPW}}$ | Minimum pulse width for clear and preset | *(2)* | 2.5 | | 3.0 | | 4.0 | | 6.0 | | ns |
| $\mathbf{t_{ODH}}$ | Output data hold time after clock | C1 = 35 pF *(3)* | 1.0 | | 1.0 | | 1.0 | | 1.0 | | ns |
| $\mathbf{t_{CNT}}$ | Minimum global clock period | | | 6.7 | | 8.2 | | 10.0 | | 13.0 | ns |
| $\mathbf{f_{CNT}}$ | Maximum internal global clock frequency | *(4)* | 149.3 | | 122.0 | | 100.0 | | 76.9 | | MHz |

*Table 30. EPM7160S External Timing Parameters (Part 2 of 2)* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | -6 | | -7 | | -10 | | -15 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{ACNT}$ | Minimum array clock period | | | 6.7 | | 8.2 | | 10.0 | | 13.0 | ns |
| $f_{ACNT}$ | Maximum internal array clock frequency | *(4)* | 149.3 | | 122.0 | | 100.0 | | 76.9 | | MHz |
| $f_{MAX}$ | Maximum clock frequency | *(5)* | 166.7 | | 166.7 | | 125.0 | | 100.0 | | MHz |

*Table 31. EPM7160S Internal Timing Parameters (Part 1 of 2)* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | -6 | | -7 | | -10 | | -15 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{IN}$ | Input pad and buffer delay | | | 0.2 | | 0.3 | | 0.5 | | 2.0 | ns |
| $t_{IO}$ | I/O input pad and buffer delay | | | 0.2 | | 0.3 | | 0.5 | | 2.0 | ns |
| $t_{FIN}$ | Fast input delay | | | 2.6 | | 3.2 | | 1.0 | | 2.0 | ns |
| $t_{SEXP}$ | Shared expander delay | | | 3.6 | | 4.3 | | 5.0 | | 8.0 | ns |
| $t_{PEXP}$ | Parallel expander delay | | | 1.0 | | 1.3 | | 0.8 | | 1.0 | ns |
| $t_{LAD}$ | Logic array delay | | | 2.8 | | 3.4 | | 5.0 | | 6.0 | ns |
| $t_{LAC}$ | Logic control array delay | | | 2.8 | | 3.4 | | 5.0 | | 6.0 | ns |
| $t_{IOE}$ | Internal output enable delay | | | 0.7 | | 0.9 | | 2.0 | | 3.0 | ns |
| $t_{OD1}$ | Output buffer and pad delay | C1 = 35 pF | | 0.4 | | 0.5 | | 1.5 | | 4.0 | ns |
| $t_{OD2}$ | Output buffer and pad delay | C1 = 35 pF *(6)* | | 0.9 | | 1.0 | | 2.0 | | 5.0 | ns |
| $t_{OD3}$ | Output buffer and pad delay | C1 = 35 pF | | 5.4 | | 5.5 | | 5.5 | | 8.0 | ns |
| $t_{ZX1}$ | Output buffer enable delay | C1 = 35 pF | | 4.0 | | 4.0 | | 5.0 | | 6.0 | ns |
| $t_{ZX2}$ | Output buffer enable delay | C1 = 35 pF *(6)* | | 4.5 | | 4.5 | | 5.5 | | 7.0 | ns |
| $t_{ZX3}$ | Output buffer enable delay | C1 = 35 pF | | 9.0 | | 9.0 | | 9.0 | | 10.0 | ns |
| $t_{XZ}$ | Output buffer disable delay | C1 = 5 pF | | 4.0 | | 4.0 | | 5.0 | | 6.0 | ns |
| $t_{SU}$ | Register setup time | | 1.0 | | 1.2 | | 2.0 | | 4.0 | | ns |
| $t_{H}$ | Register hold time | | 1.6 | | 2.0 | | 3.0 | | 4.0 | | ns |
| $t_{FSU}$ | Register setup time of fast input | | 1.9 | | 2.2 | | 3.0 | | 2.0 | | ns |
| $t_{FH}$ | Register hold time of fast input | | 0.6 | | 0.8 | | 0.5 | | 1.0 | | ns |
| $t_{RD}$ | Register delay | | | 1.3 | | 1.6 | | 2.0 | | 1.0 | ns |
| $t_{COMB}$ | Combinatorial delay | | | 1.0 | | 1.3 | | 2.0 | | 1.0 | ns |
| $t_{IC}$ | Array clock delay | | | 2.9 | | 3.5 | | 5.0 | | 6.0 | ns |
| $t_{EN}$ | Register enable time | | | 2.8 | | 3.4 | | 5.0 | | 6.0 | ns |
| $t_{GLOB}$ | Global control delay | | | 2.0 | | 2.4 | | 1.0 | | 1.0 | ns |

*Table 31. EPM7160S Internal Timing Parameters (Part 2 of 2)* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | -6 | | -7 | | -10 | | -15 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{PRE}$ | Register preset time | | | 2.4 | | 3.0 | | 3.0 | | 4.0 | ns |
| $t_{CLR}$ | Register clear time | | | 2.4 | | 3.0 | | 3.0 | | 4.0 | ns |
| $t_{PIA}$ | PIA delay | *(7)* | | 1.6 | | 2.0 | | 1.0 | | 2.0 | ns |
| $t_{LPA}$ | Low-power adder | *(8)* | | 11.0 | | 10.0 | | 11.0 | | 13.0 | ns |

*Notes to tables:*

(1) These values are specified under the recommended operating conditions shown in Table 11. See Figure 13 for more information on switching waveforms.
(2) This minimum pulse width for preset and clear applies for both global clear and array controls. The $t_{LPA}$ parameter must be added to this minimum width if the clear or reset signal incorporates the $t_{LAD}$ parameter into the signal path.
(3) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
(4) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
(5) The $\mathbf{f_{MAX}}$ values represent the highest frequency for pipelined data.
(6) Operating conditions: $V_{CCIO}$ = 3.3 V ± 10% for commercial and industrial use.
(7) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
(8) The $t_{LPA}$ parameter must be added to the $t_{LAD}$, $t_{LAC}$, $t_{IC}$, $t_{EN}$, $t_{SEXP}$, $\mathbf{t_{ACL}}$, and $\mathbf{t_{CPPW}}$ parameters for macrocells running in the low-power mode.

Tables 32 and 33 show the EPM7192S AC operating conditions.

*Table 32. EPM7192S External Timing Parameters (Part 1 of 2)* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | -7 | | -10 | | -15 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $\mathbf{t_{PD1}}$ | Input to non-registered output | C1 = 35 pF | | 7.5 | | 10.0 | | 15.0 | ns |
| $\mathbf{t_{PD2}}$ | I/O input to non-registered output | C1 = 35 pF | | 7.5 | | 10.0 | | 15.0 | ns |
| $\mathbf{t_{SU}}$ | Global clock setup time | | 4.1 | | 7.0 | | 11.0 | | ns |
| $\mathbf{t_{H}}$ | Global clock hold time | | 0.0 | | 0.0 | | 0.0 | | ns |
| $\mathbf{t_{FSU}}$ | Global clock setup time of fast input | | 3.0 | | 3.0 | | 3.0 | | ns |
| $\mathbf{t_{FH}}$ | Global clock hold time of fast input | | 0.0 | | 0.5 | | 0.0 | | ns |
| $\mathbf{t_{CO1}}$ | Global clock to output delay | C1 = 35 pF | | 4.7 | | 5.0 | | 8.0 | ns |
| $\mathbf{t_{CH}}$ | Global clock high time | | 3.0 | | 4.0 | | 5.0 | | ns |

*Table 32. EPM7192S External Timing Parameters (Part 2 of 2)* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | -7 | | -10 | | -15 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{CL}$ | Global clock low time | | 3.0 | | 4.0 | | 5.0 | | ns |
| $t_{ASU}$ | Array clock setup time | | 1.0 | | 2.0 | | 4.0 | | ns |
| $t_{AH}$ | Array clock hold time | | 1.8 | | 3.0 | | 4.0 | | ns |
| $t_{ACO1}$ | Array clock to output delay | C1 = 35 pF | | 7.8 | | 10.0 | | 15.0 | ns |
| $t_{ACH}$ | Array clock high time | | 3.0 | | 4.0 | | 6.0 | | ns |
| $t_{ACL}$ | Array clock low time | | 3.0 | | 4.0 | | 6.0 | | ns |
| $t_{CPPW}$ | Minimum pulse width for clear and preset | *(2)* | 3.0 | | 4.0 | | 6.0 | | ns |
| $t_{ODH}$ | Output data hold time after clock | C1 = 35 pF *(3)* | 1.0 | | 1.0 | | 1.0 | | ns |
| $t_{CNT}$ | Minimum global clock period | | | 8.0 | | 10.0 | | 13.0 | ns |
| $f_{CNT}$ | Maximum internal global clock frequency | *(4)* | 125.0 | | 100.0 | | 76.9 | | MHz |
| $t_{ACNT}$ | Minimum array clock period | | | 8.0 | | 10.0 | | 13.0 | ns |
| $f_{ACNT}$ | Maximum internal array clock frequency | *(4)* | 125.0 | | 100.0 | | 76.9 | | MHz |
| $f_{MAX}$ | Maximum clock frequency | *(5)* | 166.7 | | 125.0 | | 100.0 | | MHz |

*Table 33. EPM7192S Internal Timing Parameters (Part 1 of 2)* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | -7 | | -10 | | -15 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{IN}$ | Input pad and buffer delay | | | 0.3 | | 0.5 | | 2.0 | ns |
| $t_{IO}$ | I/O input pad and buffer delay | | | 0.3 | | 0.5 | | 2.0 | ns |
| $t_{FIN}$ | Fast input delay | | | 3.2 | | 1.0 | | 2.0 | ns |
| $t_{SEXP}$ | Shared expander delay | | | 4.2 | | 5.0 | | 8.0 | ns |
| $t_{PEXP}$ | Parallel expander delay | | | 1.2 | | 0.8 | | 1.0 | ns |
| $t_{LAD}$ | Logic array delay | | | 3.1 | | 5.0 | | 6.0 | ns |
| $t_{LAC}$ | Logic control array delay | | | 3.1 | | 5.0 | | 6.0 | ns |
| $t_{IOE}$ | Internal output enable delay | | | 0.9 | | 2.0 | | 3.0 | ns |
| $t_{OD1}$ | Output buffer and pad delay | C1 = 35 pF | | 0.5 | | 1.5 | | 4.0 | ns |
| $t_{OD2}$ | Output buffer and pad delay | C1 = 35 pF *(6)* | | 1.0 | | 2.0 | | 5.0 | ns |
| $t_{OD3}$ | Output buffer and pad delay | C1 = 35 pF | | 5.5 | | 5.5 | | 7.0 | ns |
| $t_{ZX1}$ | Output buffer enable delay | C1 = 35 pF | | 4.0 | | 5.0 | | 6.0 | ns |
| $t_{ZX2}$ | Output buffer enable delay | C1 = 35 pF *(6)* | | 4.5 | | 5.5 | | 7.0 | ns |
| $t_{ZX3}$ | Output buffer enable delay | C1 = 35 pF | | 9.0 | | 9.0 | | 10.0 | ns |

*Table 33. EPM7192S Internal Timing Parameters (Part 2 of 2)* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | -7 | | -10 | | -15 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{XZ}$ | Output buffer disable delay | C1 = 5 pF | | 4.0 | | 5.0 | | 6.0 | ns |
| $t_{SU}$ | Register setup time | | 1.1 | | 2.0 | | 4.0 | | ns |
| $t_{H}$ | Register hold time | | 1.7 | | 3.0 | | 4.0 | | ns |
| $t_{FSU}$ | Register setup time of fast input | | 2.3 | | 3.0 | | 2.0 | | ns |
| $t_{FH}$ | Register hold time of fast input | | 0.7 | | 0.5 | | 1.0 | | ns |
| $t_{RD}$ | Register delay | | | 1.4 | | 2.0 | | 1.0 | ns |
| $t_{COMB}$ | Combinatorial delay | | | 1.2 | | 2.0 | | 1.0 | ns |
| $t_{IC}$ | Array clock delay | | | 3.2 | | 5.0 | | 6.0 | ns |
| $t_{EN}$ | Register enable time | | | 3.1 | | 5.0 | | 6.0 | ns |
| $t_{GLOB}$ | Global control delay | | | 2.5 | | 1.0 | | 1.0 | ns |
| $t_{PRE}$ | Register preset time | | | 2.7 | | 3.0 | | 4.0 | ns |
| $t_{CLR}$ | Register clear time | | | 2.7 | | 3.0 | | 4.0 | ns |
| $t_{PIA}$ | PIA delay | *(7)* | | 2.4 | | 1.0 | | 2.0 | ns |
| $t_{LPA}$ | Low-power adder | *(8)* | | 10.0 | | 11.0 | | 13.0 | ns |

*Notes to tables:*

(1) These values are specified under the recommended operating conditions shown in Table 11. See Figure 13 for more information on switching waveforms.

(2) This minimum pulse width for preset and clear applies for both global clear and array controls. The $t_{LPA}$ parameter must be added to this minimum width if the clear or reset signal incorporates the $t_{LAD}$ parameter into the signal path.

(3) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.

(4) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.

(5) The $\mathbf{f_{MAX}}$ values represent the highest frequency for pipelined data.

(6) Operating conditions: $V_{CCIO}$ = 3.3 V ± 10% for commercial and industrial use.

(7) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.

(8) The $t_{LPA}$ parameter must be added to the $t_{LAD}$, $t_{LAC}$, $t_{IC}$, $t_{EN}$, $t_{SEXP}$, $\mathbf{t_{ACL}}$, and $\mathbf{t_{CPPW}}$ parameters for macrocells running in the low-power mode.

Tables 34 and 35 show the EPM7256S AC operating conditions.

**Table 34. EPM7256S External Timing Parameters** *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | -7 | | -10 | | -15 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{PD1}$ | Input to non-registered output | C1 = 35 pF | | 7.5 | | 10.0 | | 15.0 | ns |
| $t_{PD2}$ | I/O input to non-registered output | C1 = 35 pF | | 7.5 | | 10.0 | | 15.0 | ns |
| $t_{SU}$ | Global clock setup time | | 3.9 | | 7.0 | | 11.0 | | ns |
| $t_{H}$ | Global clock hold time | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{FSU}$ | Global clock setup time of fast input | | 3.0 | | 3.0 | | 3.0 | | ns |
| $t_{FH}$ | Global clock hold time of fast input | | 0.0 | | 0.5 | | 0.0 | | ns |
| $t_{CO1}$ | Global clock to output delay | C1 = 35 pF | | 4.7 | | 5.0 | | 8.0 | ns |
| $t_{CH}$ | Global clock high time | | 3.0 | | 4.0 | | 5.0 | | ns |
| $t_{CL}$ | Global clock low time | | 3.0 | | 4.0 | | 5.0 | | ns |
| $t_{ASU}$ | Array clock setup time | | 0.8 | | 2.0 | | 4.0 | | ns |
| $t_{AH}$ | Array clock hold time | | 1.9 | | 3.0 | | 4.0 | | ns |
| $t_{ACO1}$ | Array clock to output delay | C1 = 35 pF | | 7.8 | | 10.0 | | 15.0 | ns |
| $t_{ACH}$ | Array clock high time | | 3.0 | | 4.0 | | 6.0 | | ns |
| $t_{ACL}$ | Array clock low time | | 3.0 | | 4.0 | | 6.0 | | ns |
| $t_{CPPW}$ | Minimum pulse width for clear and preset | *(2)* | 3.0 | | 4.0 | | 6.0 | | ns |
| $t_{ODH}$ | Output data hold time after clock | C1 = 35 pF *(3)* | 1.0 | | 1.0 | | 1.0 | | ns |
| $t_{CNT}$ | Minimum global clock period | | | 7.8 | | 10.0 | | 13.0 | ns |
| $f_{CNT}$ | Maximum internal global clock frequency | *(4)* | 128.2 | | 100.0 | | 76.9 | | MHz |
| $t_{ACNT}$ | Minimum array clock period | | | 7.8 | | 10.0 | | 13.0 | ns |
| $f_{ACNT}$ | Maximum internal array clock frequency | *(4)* | 128.2 | | 100.0 | | 76.9 | | MHz |
| $f_{MAX}$ | Maximum clock frequency | *(5)* | 166.7 | | 125.0 | | 100.0 | | MHz |

*Table 35. EPM7256S Internal Timing Parameters* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | -7 | | -10 | | -15 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{IN}$ | Input pad and buffer delay | | | 0.3 | | 0.5 | | 2.0 | ns |
| $t_{IO}$ | I/O input pad and buffer delay | | | 0.3 | | 0.5 | | 2.0 | ns |
| $t_{FIN}$ | Fast input delay | | | 3.4 | | 1.0 | | 2.0 | ns |
| $t_{SEXP}$ | Shared expander delay | | | 3.9 | | 5.0 | | 8.0 | ns |
| $t_{PEXP}$ | Parallel expander delay | | | 1.1 | | 0.8 | | 1.0 | ns |
| $t_{LAD}$ | Logic array delay | | | 2.6 | | 5.0 | | 6.0 | ns |
| $t_{LAC}$ | Logic control array delay | | | 2.6 | | 5.0 | | 6.0 | ns |
| $t_{IOE}$ | Internal output enable delay | | | 0.8 | | 2.0 | | 3.0 | ns |
| $t_{OD1}$ | Output buffer and pad delay | C1 = 35 pF | | 0.5 | | 1.5 | | 4.0 | ns |
| $t_{OD2}$ | Output buffer and pad delay | C1 = 35 pF *(6)* | | 1.0 | | 2.0 | | 5.0 | ns |
| $t_{OD3}$ | Output buffer and pad delay | C1 = 35 pF | | 5.5 | | 5.5 | | 8.0 | ns |
| $t_{ZX1}$ | Output buffer enable delay | C1 = 35 pF | | 4.0 | | 5.0 | | 6.0 | ns |
| $t_{ZX2}$ | Output buffer enable delay | C1 = 35 pF *(6)* | | 4.5 | | 5.5 | | 7.0 | ns |
| $t_{ZX3}$ | Output buffer enable delay | C1 = 35 pF | | 9.0 | | 9.0 | | 10.0 | ns |
| $t_{XZ}$ | Output buffer disable delay | C1 = 5 pF | | 4.0 | | 5.0 | | 6.0 | ns |
| $t_{SU}$ | Register setup time | | 1.1 | | 2.0 | | 4.0 | | ns |
| $t_{H}$ | Register hold time | | 1.6 | | 3.0 | | 4.0 | | ns |
| $t_{FSU}$ | Register setup time of fast input | | 2.4 | | 3.0 | | 2.0 | | ns |
| $t_{FH}$ | Register hold time of fast input | | 0.6 | | 0.5 | | 1.0 | | ns |
| $t_{RD}$ | Register delay | | | 1.1 | | 2.0 | | 1.0 | ns |
| $t_{COMB}$ | Combinatorial delay | | | 1.1 | | 2.0 | | 1.0 | ns |
| $t_{IC}$ | Array clock delay | | | 2.9 | | 5.0 | | 6.0 | ns |
| $t_{EN}$ | Register enable time | | | 2.6 | | 5.0 | | 6.0 | ns |
| $t_{GLOB}$ | Global control delay | | | 2.8 | | 1.0 | | 1.0 | ns |
| $t_{PRE}$ | Register preset time | | | 2.7 | | 3.0 | | 4.0 | ns |
| $t_{CLR}$ | Register clear time | | | 2.7 | | 3.0 | | 4.0 | ns |
| $t_{PIA}$ | PIA delay | *(7)* | | 3.0 | | 1.0 | | 2.0 | ns |
| $t_{LPA}$ | Low-power adder | *(8)* | | 10.0 | | 11.0 | | 13.0 | ns |

*Notes to tables:*

(1) These values are specified under the recommended operating conditions shown in Table 11. See Figure 13 for more information on switching waveforms.
(2) This minimum pulse width for preset and clear applies for both global clear and array controls. The $t_{LPA}$ parameter must be added to this minimum width if the clear or reset signal incorporates the $t_{LAD}$ parameter into the signal path.
(3) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
(4) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
(5) The $\mathbf{f_{MAX}}$ values represent the highest frequency for pipelined data.
(6) Operating conditions: $V_{CCIO} = 3.3\ V \pm 10\%$ for commercial and industrial use.
(7) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
(8) The $t_{LPA}$ parameter must be added to the $t_{LAD}$, $t_{LAC}$, $t_{IC}$, $t_{EN}$, $t_{SEXP}$, $\mathbf{t_{ACL}}$, and $\mathbf{t_{CPPW}}$ parameters for macrocells running in the low-power mode.

## Power Consumption

Supply power (P) versus frequency ($\mathbf{f_{MAX}}$ in MHz) for MAX 7000 devices is calculated with the following equation:

$$P = P_{INT} + P_{IO} = I_{CCINT} \times V_{CC} + P_{IO}$$

The $P_{IO}$ value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)*.

The $I_{CCINT}$ value, which depends on the switching frequency and the application logic, is calculated with the following equation:

$$I_{CCINT} =$$

$$A \times MC_{TON} + B \times (MC_{DEV} - MC_{TON}) + C \times MC_{USED} \times \mathbf{f_{MAX}} \times \mathbf{tog_{LC}}$$

The parameters in this equation are shown below:

| | | |
|---|---|---|
| $MC_{TON}$ | = | Number of macrocells with the Turbo Bit option turned on, as reported in the MAX+PLUS II Report File (**.rpt**) |
| $MC_{DEV}$ | = | Number of macrocells in the device |
| $MC_{USED}$ | = | Total number of macrocells in the design, as reported in the MAX+PLUS II Report File (**.rpt**) |
| $\mathbf{f_{MAX}}$ | = | Highest clock frequency to the device |
| $\mathbf{tog_{LC}}$ | = | Average ratio of logic cells toggling at each clock (typically 0.125) |
| A, B, C | = | Constants, shown in Table 36 |

*Table 36. MAX 7000 $I_{CC}$ Equation Constants*

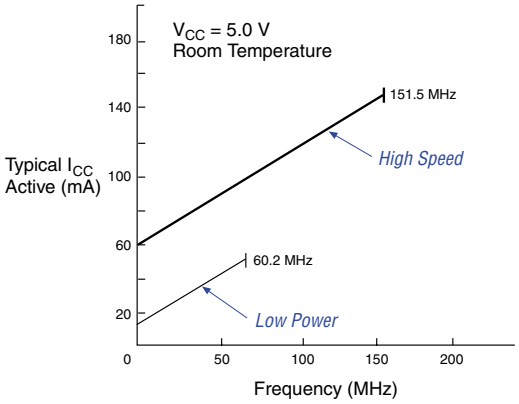
| Device | A | B | C |
|---|---|---|---|
| EPM7032 | 1.87 | 0.52 | 0.144 |
| EPM7064 | 1.63 | 0.74 | 0.144 |
| EPM7096 | 1.63 | 0.74 | 0.144 |
| EPM7128E | 1.17 | 0.54 | 0.096 |
| EPM7160E | 1.17 | 0.54 | 0.096 |
| EPM7192E | 1.17 | 0.54 | 0.096 |
| EPM7256E | 1.17 | 0.54 | 0.096 |
| EPM7032S | 0.93 | 0.40 | 0.040 |
| EPM7064S | 0.93 | 0.40 | 0.040 |
| EPM7128S | 0.93 | 0.40 | 0.040 |
| EPM7160S | 0.93 | 0.40 | 0.040 |
| EPM7192S | 0.93 | 0.40 | 0.040 |
| EPM7256S | 0.93 | 0.40 | 0.040 |

This calculation provides an $I_{CC}$ estimate based on typical conditions using a pattern of a 16-bit, loadable, enabled, up/down counter in each LAB with no output load. Actual $I_{CC}$ values should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

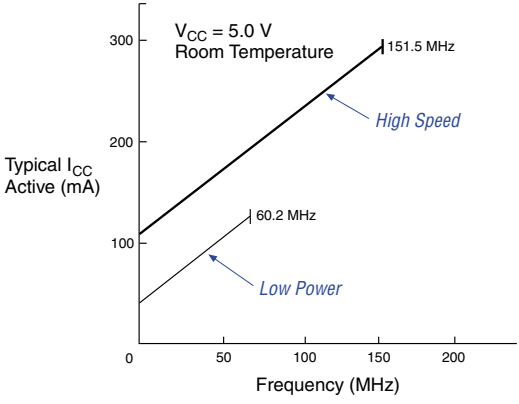
Figure 14 shows typical supply current versus frequency for MAX 7000 devices.

*Figure 14. $I_{CC}$ vs. Frequency for MAX 7000 Devices (Part 1 of 2)*

**EPM7032**




**EPM7064**




**EPM7096**

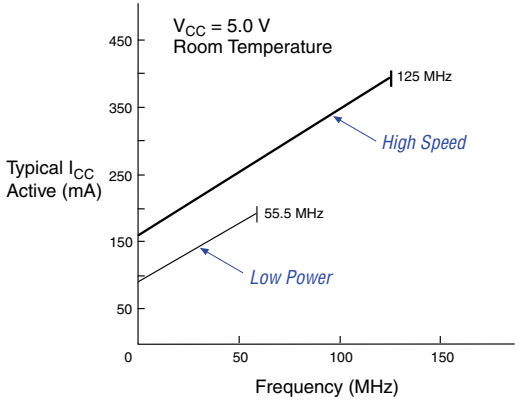


*Figure 14. $I_{CC}$ vs. Frequency for MAX 7000 Devices (Part 2 of 2)*

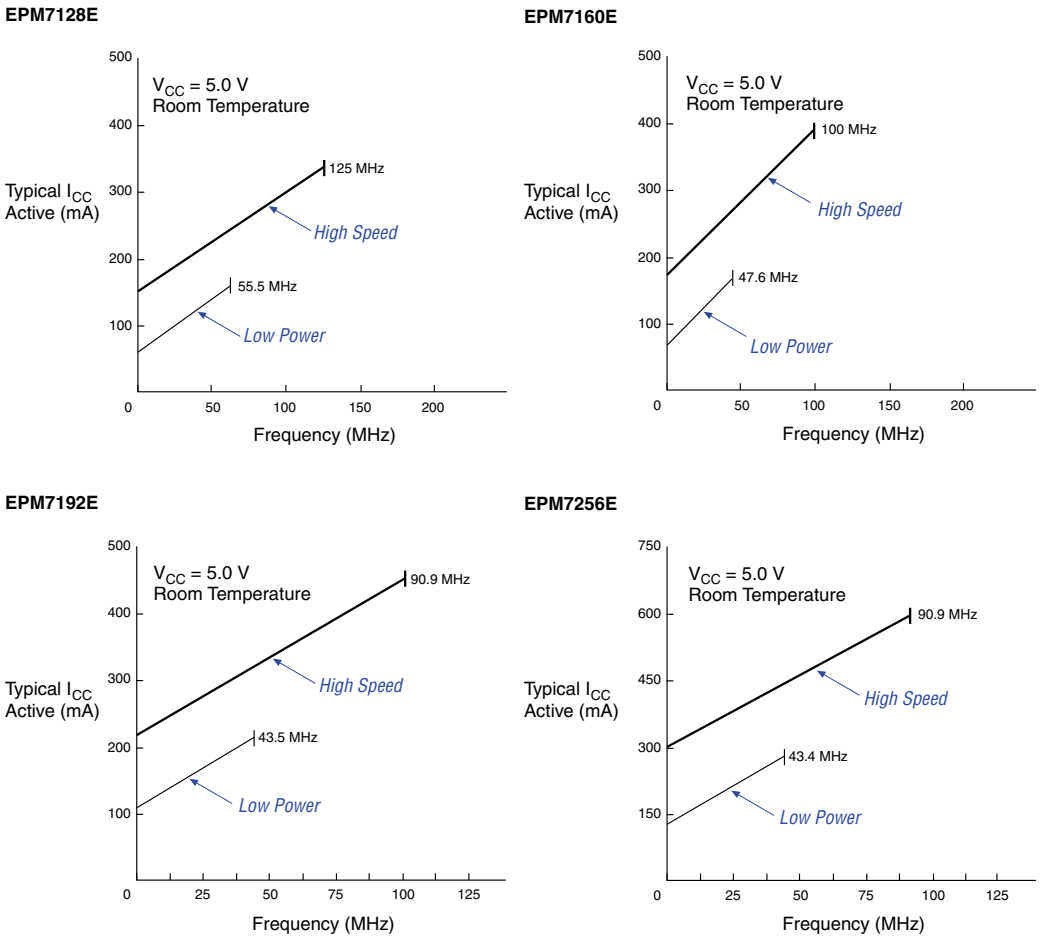


Figure 15 shows typical supply current versus frequency for MAX 7000S devices.

*Figure 15. $I_{CC}$ vs. Frequency for MAX 7000S Devices (Part 1 of 2)*

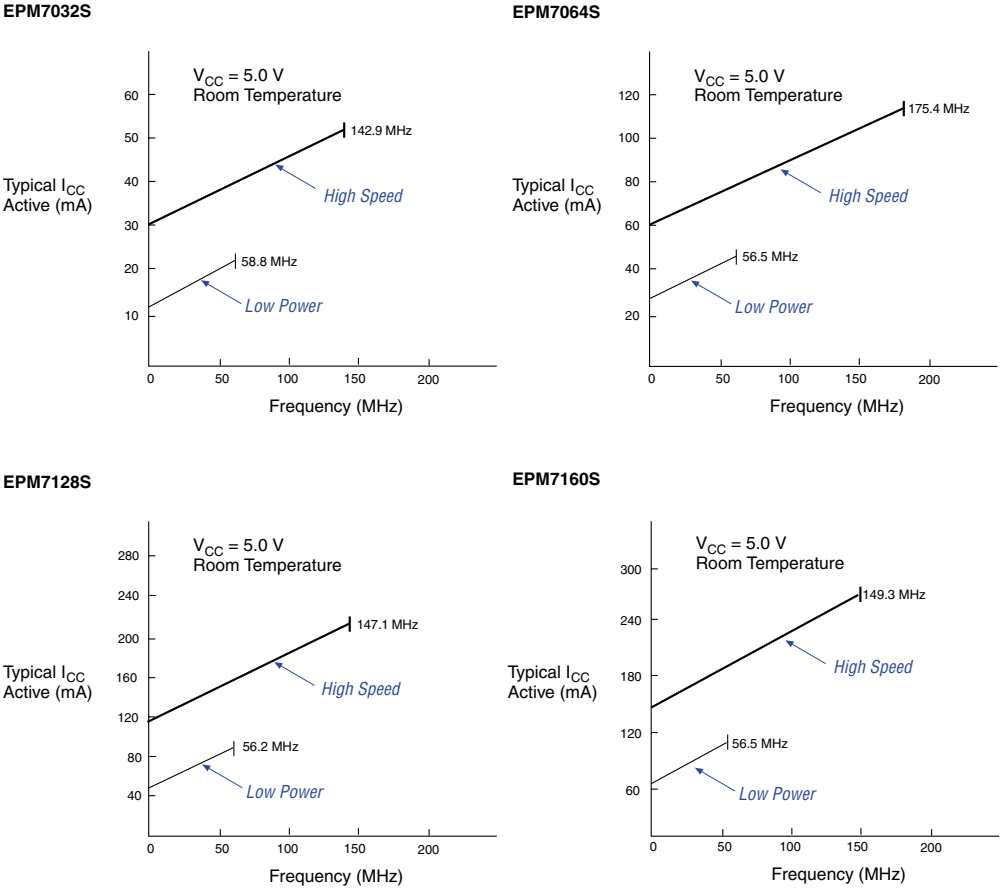
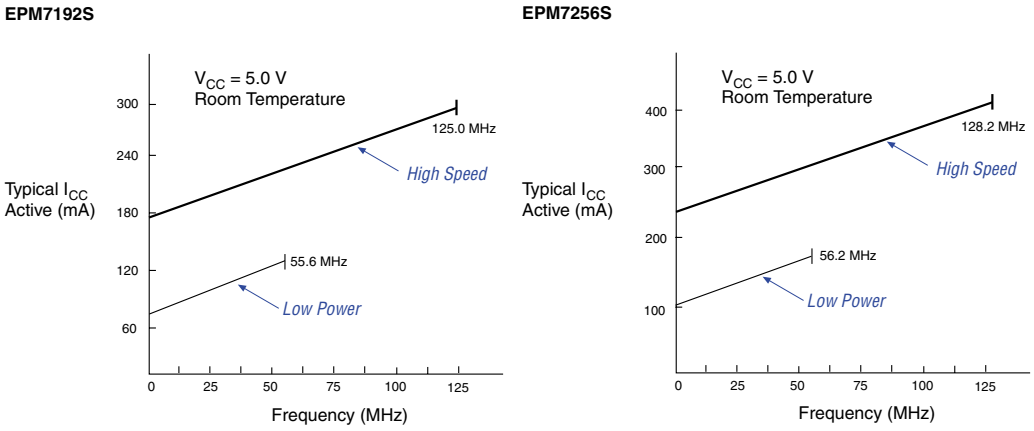


*Figure 15. $I_{CC}$ vs. Frequency for MAX 7000S Devices (Part 2 of 2)*



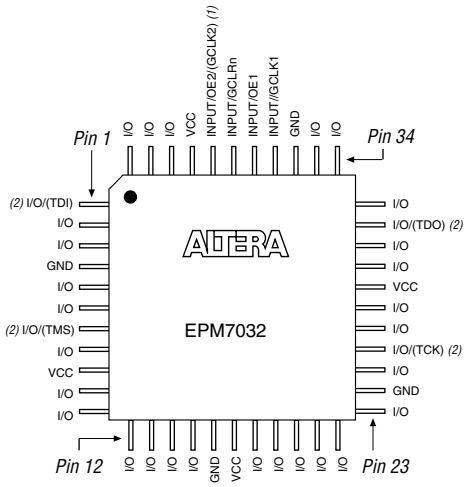

## Device Pin-Outs

See the Altera web site (**http://www.altera.com**) or the *Altera Digital Library* for pin-out information.

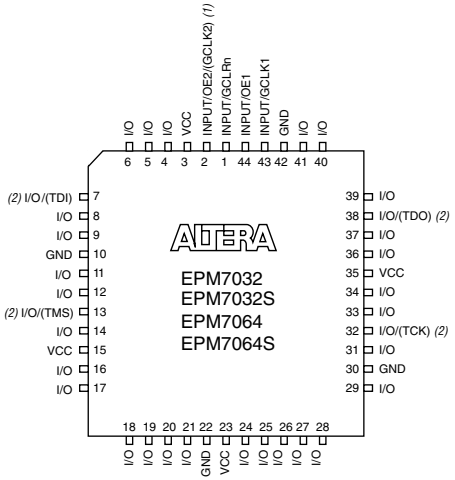
Figures 16 through 22 show the package pin-out diagrams for MAX 7000 devices.

***Figure 16. 44-Pin Package Pin-Out Diagram***

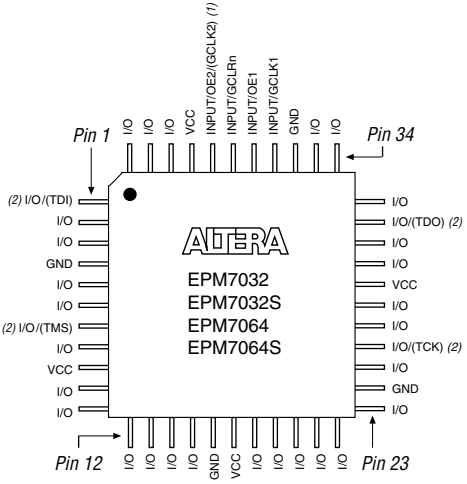
*Package outlines not drawn to scale.*




44-Pin PQFP




44-Pin PLCC

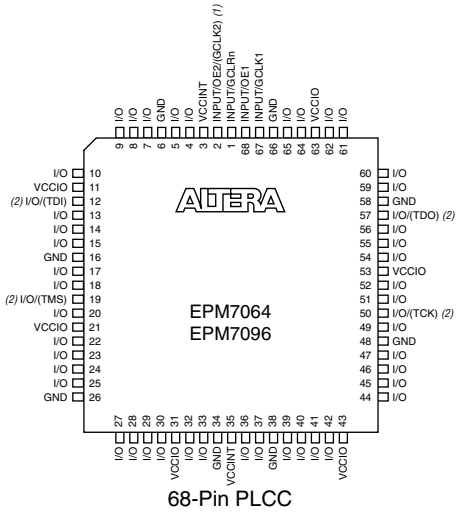



44-Pin TQFP

*Notes:*
(1) The pin functions shown in parenthesis are only available in MAX 7000E and MAX 7000S devices.
(2) JTAG ports are available in MAX 7000S devices only.

*Figure 17. 68-Pin Package Pin-Out Diagram*

*Package outlines not drawn to scale.*



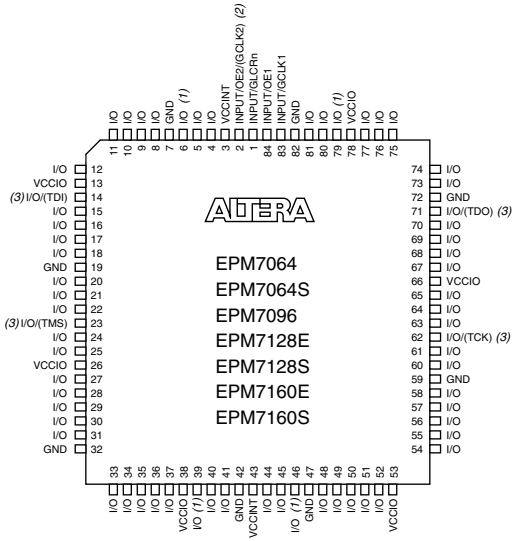

*Notes:*

(1) The pin functions shown in parenthesis are only available in MAX 7000E and MAX 7000S devices.

(2) JTAG ports are available in MAX 7000S devices only.

### *Figure 18. 84-Pin Package Pin-Out Diagram*

*Package outline not drawn to scale.*

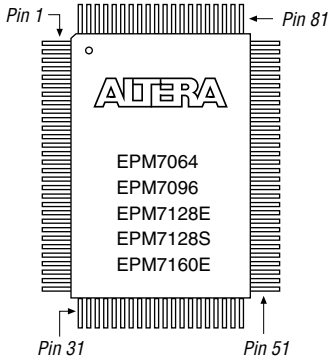



84-Pin PLCC

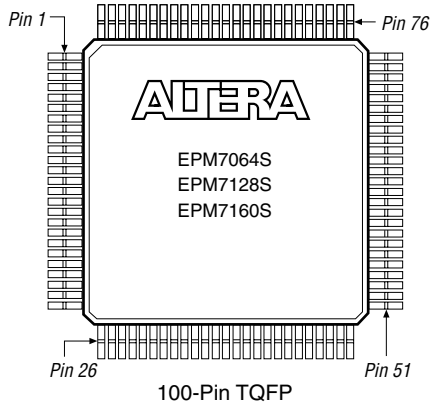
*Notes:*
(1) Pins 6, 39, 46, and 79 are no-connect (N.C.) pins on EPM7096, EPM7160E, and EPM7160S devices.
(2) The pin functions shown in parenthesis are only available in MAX 7000E and MAX 7000S devices.
(3) JTAG ports are available in MAX 7000S devices only.

*Figure 19. 100-Pin Package Pin-Out Diagram*

*Package outline not drawn to scale.*



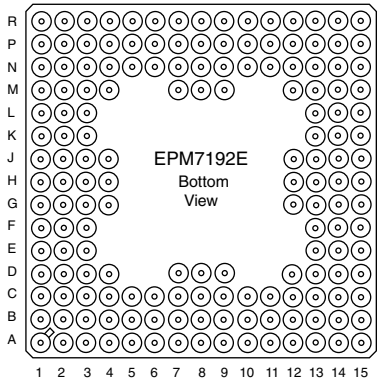

100-Pin PQFP



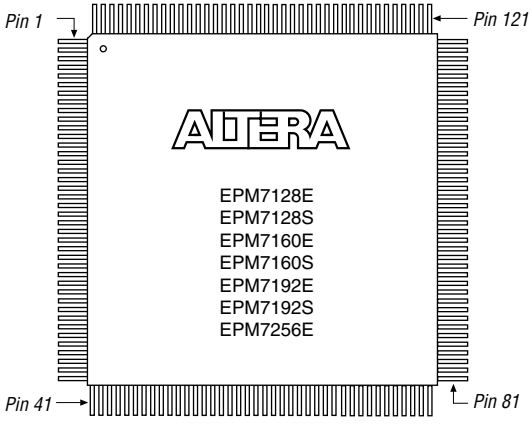

100-Pin TQFP

*Figure 20. 160-Pin Package Pin-Out Diagram*

*Package outline not drawn to scale.*



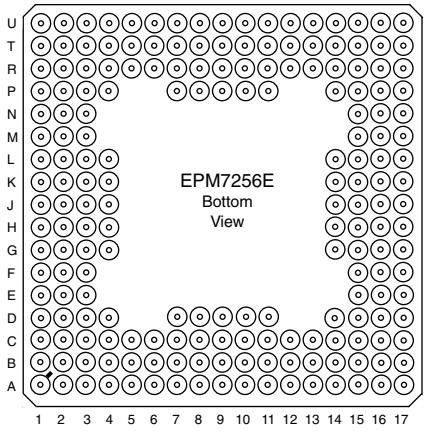

160-Pin PGA




160-Pin PQFP

### *Figure 21. 192-Pin Package Pin-Out Diagram*

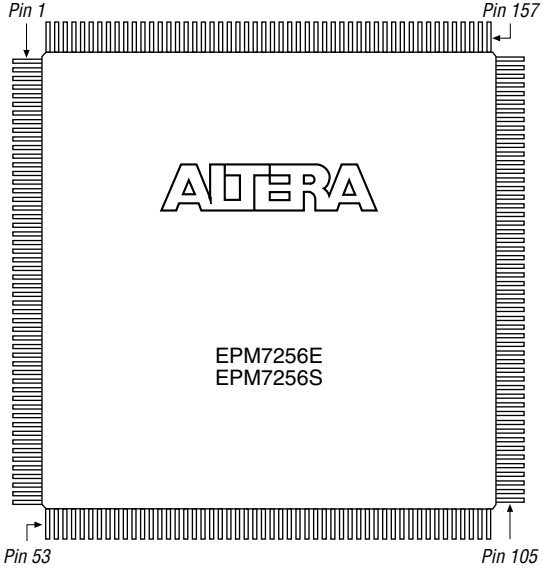
*Package outline not drawn to scale.*




192-Pin PGA

### *Figure 22. 208-Pin Package Pin-Out Diagram*

*Package outline not drawn to scale.*




208-Pin PQFP/RQFP

## Revision History

The information contained in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.2 supersedes information published in previous versions. The following changes were made in the *MAX 3000A Programmable Logic Device Family Data Sheet* version 6.2:

- Updated leakage current information in Table 12.
- Added *Note (1)* to Tables 16 – 23, 24 – 25, 26 – 27, 28 – 29, 30 – 31, 32 – 33, and 34 – 35.

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