TEXAS INSTRUMENTS
SN6507
SLLSFM0 – MARCH 2022

SN6507 Low-Emission 36V Push-Pull Transformer Driver with Duty Cycle Control for Isolated Power Supplies

1 Features

- Push-pull driver for transformers
- Wide input voltage range: 3 V to 36 V
  - 60 V input voltage tolerance
  - Duty-cycle control for line regulation
- 0.5 A switches with programmable current limit
- Wide switching frequency range: 150 kHz to 2 MHz
  - Allows small-size transformers
  - Programmable switching frequency
  - External clock synchronization option
- Ultra-low noise and EMI
  - Symmetric push-pull topology
  - Spread sprectrum clocking
  - Pin-configurable slew-rate control
- Protection Features
  - Adjustable under voltage lockout (UVLO)
  - Programmable over-current protection (OCP)
  - Over voltage lockout (OVLO)
  - Thermal shutdown (TSD)
- Wide temperature range: –55°C to 125°C
- Programmable soft-start to reduce In-rush current
- 10-Pin HVSSOP (DGQ) package with thermal pad

2 Applications

- Solar Inverters, Protection Relays
- Factory Automation
- Building Automation
- Medical instruments
- Motor Drives: IGBT and SiC Gate Driver Supplies
- Isolated power supply for CAN, RS-485, RS-422, RS-232, SPI, I2C, low-power LAN

3 Description

The SN6507 is a high voltage, high frequency push-pull transformer driver providing isolated power in a small solution size. The device comes with the push-pull topology's benefits of simplicity, low EMI, and flux cancellation to prevent transformer saturation. Further space savings are achieved through duty-cycle control, which reduces component count for wide-input ranges, and by selecting a high switching frequency, reducing the size of the transformer.

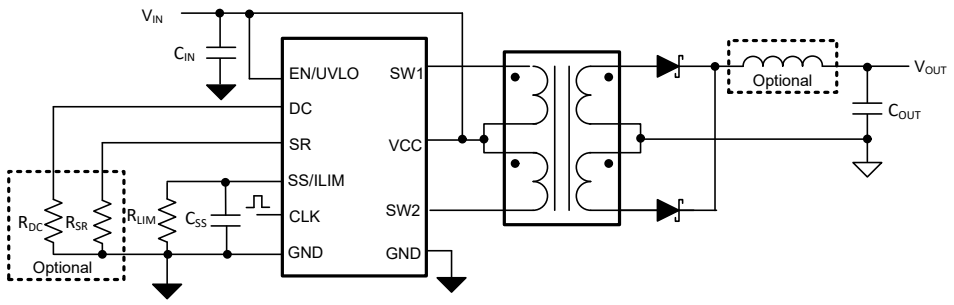
The device integrates the controller and two 0.5-A NMOS power switches that switch out of phase. Its input operating range is programmed with precision undervoltage lockouts. The device is protected from fault conditions by over-current protection (OCP), adjustable under-voltage lockout (UVLO), over voltage lockout (OVLO), thermal shutdown (TSD), and break-before-make circuitry.

The programmable Soft Start (SS) minimizes inrush currents and provides power supply sequencing for critical power up requirements. Spread Spectrum Clocking (SSC) and pin-configurable scalable Slew Rate Control (SRC) further reduces emissions for ultra-low EMI requirements.

The SN6507 is available in a 10-pin HVSSOP DGQ package. The device operation is characterized for a temperature range from –55°C to 125°C.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN6507	HVSSOP (10 Pin)	3 mm × 3 mm



Simplified Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
March 2022	*	Initial Release

5 Pin Configuration and Functions

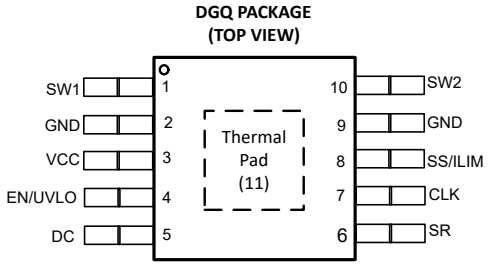

Figure 5-1. DGQ Package HVSSOP (10 Pin) Top View

Table 5-1. Pin Functions

PIN			DESCRIPTION
NAME	NO.	TYPE	
SW1	1	O	Open drain output of the first power MOSFET. Typically connected to either of the outer terminals of the center tap transformer. Because large currents flow through these pins, their external traces should be kept short.
GND	2	P	Ground connection of internal control circuits and power MOSFET. Pin 2 and Pin 9 must be shorted on PCB for optimzed emissions and efficiency.
VCC	3	P	The VCC pin is the main supply pin for the power and analog circuits. Short duration, high current pulses are produced during the turn on and turn off of the power switches.
EN/UVLO	4	I	Enable input and undervoltage lockout (UVLO) programming pin. • If the pin voltage is above EN_UVLO threshold , the part is enabled and will start switching when VCC is above VCC_UVLO threshold. • If the pin is shorted to VCC, the part is self-started when VCC is above VCC_UVLO threshold. • If the pin is floating, or the pin voltage is below EN_UVLO threshold, the device stops switching.
DC	5	I	Duty cycle control pin to compensate input variation. A resistor on this pin to GND sets the duty cycle. If unused, leave the pin floating, the duty cycle is set to the default value (48%). Duty cyle control is disabled in SYNC mode .
SR	6	I	Slew rate control pin to further optimize emission performance. This pin adjusts slew rate of SW1 and SW2 by connecting a resistor to GND. If the pin is left floating, the part switches at the default slew rates.
CLK	7	I	This pin is used to sync the device with an external clock (SYNC mode), or program the switching frequency by connecting the pin to ground through a resistor. If shorted to GND, the part will switch at default frequency (1MHz typical). If left floating, the part will stop switching.
SS/ILIM	8	I	Multifunction Soft-Start (SS) and Current-Limit (ILIM) input pin. • A capacitor to GND is needed to adjust the output soft-start time and input inrush current. • A resistor to GND is needed to protect the device through the programmable current limit.
GND	9	P	Ground connection of internal control circuits and power MOSFET. Pin 2 and Pin 9 must be shorted on PCB for optimized emissions and efficiency.
SW2	10	O	Open drain output of the second power MOSFET. Typically connected to either of the outer terminals of the center tap transformer. Because large currents flow through these pins, their external traces should be kept short.
PowerPAD	11	-	GND pins (Pin 2 and Pin 9) must be electrically connected to the power pad (Pin 11) on the printed circuit board for proper operation

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1). All typical values are at T_A = 25°C, V_{CC} = 24 V.

		MIN	MAX	UNIT
Supply voltage (2)	V_{CC}	–0.5	60	V
Voltage	EN/UVLO	–0.5	V_{CC} + 0.5	V
Voltage	SS/ILIM, CLK, DC	–0.5	6	V
Output switch voltage	SW1, SW2		85	V
Peak output switch current	$I_{(D1)Pk}$, $I_{(D2)Pk}$		1.6	A
Junction temperature, T_J		-55	150	°C
Storage temperature range, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operation Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods affects device reliability.
(2) All voltage values are with respect to the local ground terminal (GND) and are peak voltage values.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 3A	±4000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD Classification Level C6	±1500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

			MIN	TYP	MAX	UNIT
V_{CC}	Input Voltage		3		36	V
I_{SW1}, I_{SW2}	Output switch current - Primary side	3 V < V_{CC} < 6 V			0.4	A
		6 V < V_{CC} < 36 V			0.5	
T_A	Ambient temperature		–55		125	°C
T_J	Junction temperature		–55		150	°C
C_{SS}	Soft-start capacitor on SS/ILIM pin		0.05		10	µF
RILIM	Current limiting resistor on SS/ILIM pin		18		261	kΩ
R_{SR}	Resistor on SR pin for Slew rate control		4.8		21	kΩ
R_{CLK}	Resistor on CLK pin for programmable frequency		4		111	kΩ

6.4 Thermal Information

THERMAL METRIC(1)		SN6507 DGQ (HVSSOP) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	40	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	32	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	21.9	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case(bottom) thermal resistance	13	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Minimum and maximum limits apply over the recommended junction temperature range, unless otherwise indicated. All typical values are at T_A = 25°C, V_{CC} = 24 V, CLK F_{SW} = 1 MHz and $V_{EN/UVLO}$=2.5 V unless otherwise stated.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
SUPPLY CURRENT							
$I_{(Vcc)}$	VIN Supply Current (3 V < $V_{C\ C}$ < 36V) , not including switch drive currents	$V_{EN/UVLO}$=2.5V, R_L = 50 Ω		3	4	mA	
$I_{SHUTDOWN}$	VIN shutdown current	$V_{EN/UVLO}$=0V, R_L = 50 Ω		0.8	2.5	µA	
$I_{LKG(SS/ILIM)}$	Leakage Current on SS/ILIM pin	$V_{EN/UVLO}$=0V, Voltage of SS/ILIM = 5V			0.7	µA	
ENABLE AND UVLO							
$VCC_{UVLO-RISING}$	VCC Positive-going UVLO threshold	VCC rising , EN/UVLO is shorted to VCC		2.8	2.9	V	
$VCC_{UVLO-FALLING}$	VCC Negative-going UVLO threshold	VCC falling, EN/UVLO is shorted to VCC	2.5	2.65		V	
$VCC_{UVLO-HYS}$	VCC UVLO threshold hysteresis	EN/UVLO is shorted to VCC	0.13	0.14		V	
$EN_{UVLO-RISING}$	EN/UVLO Positive-going UVLO threshold	EN/UVLO rising	1.4	1.5	1.6	V	
$EN_{UVLO-FALLING}$	EN/UVLO Negative-going UVLO threshold	EN/UVLO falling	1.25	1.35	1.45	V	
$EN_{UVLO-HYS}$	EN/UVLO UVLO threshold hysteresis		0.14	0.15		V	
T_{EN_glitch}	EN glitch filter		5			µs	
POWER STAGE							
DMM	Average ON time mismatch between SW1 and SW2	R_L = 50 Ω		0		%	
$R_{(ON)}$	Output switch ON resistance	V_{CC} = 24 V, ISW1,ISW2 = 0.5 A		0.45	1	Ω	
$V_{(SLEW)}$	Voltage slew rates on SW1 and SW2	R_L = 50 Ω to V_{CC}, V_{CC} = 12 V; R_{SR} = 9.6 kΩ (Default), Figure 7-3		298		V/µs	
$V_{(SLEW)}$	Voltage slew rates on SW1 and SW2	R_L = 50 Ω to V_{CC}, V_{CC} = 24 V; R_{SR} = 9.6 kΩ (Default)		369		V/µs	
t_{DEAD}	Dead Time to avoid shoot through	Measured at 0.5V_{CC} with R_L = 50 Ω, F_{SW} = 1M Hz, RSR=9.6k Ω (or Default), Figure 7-2		70		ns	
CLK							
F_{SW}	D1, D2 average switching Frequency (Default)	R_L = 50 Ω, R_{CLK} = 0 kΩ, Figure 7-2	790	1000	1280	KHz	
$F_{(SYNC)}$	External clock frequency on CLK pin	Sync external clock applied on CLK pin. SW1/SW2 switches at 1/2 of the external CLK freq	200		4000	kHz	
$V_{CLK(High)}$	CLK pin logic high threshold			1.5	1.7	V	
$V_{CLK(Low)}$	CLK pin logic low threshold		1.0	1.2		V	
SOFT-START							
t_{PWRUP}	Power-up time	C_{SS} = 0 µF, From EN=High to full drive-current available at SW1 and SW2		300	400	µs	
t_{PWRDN}	Power-down time	C_{SS} = 0 µF, From EN=Low to output MOSFETs off (no current on SW1 and SW2)			10	µs	
I_{SS}	SS ext capacitor charging current			275		µA	
C_{SS} Range	SS ext capacitor range		0.05		10	µF	
CURRENT LIMIT							
I_{LIM}	SW1 and SW2 Current Limit	R_{LIM} = 18.2 kΩ	1.00	1.30	1.59	A	
I_{LIM}	SW1 and SW2 Current Limit	R_{LIM} = 261 kΩ	0.06	0.10	0.14	A	
DC CONTROL							
D_{sw1},D_{sw2}	Switching Duty Cycle on SW1 and SW2	DC pin floating (Default) F_{SW} = 300KHz, Figure 7-2		48		%	
D_{sw1},D_{sw2}	Switching Duty Cycle on SW1 and SW2	External CLK (SYNC mode) F_{SW} = 300KHz, Figure 7-2		48		%	
INPUT OVLO							
$VCC_{OVLO-RISING}$	Input Over-voltage Lockout Rising Threshold	VCC rising	36.9	38.7	40.5	V	

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Minimum and maximum limits apply over the recommended junction temperature range, unless otherwise indicated. All typical values are at T_A = 25°C, V_{CC} = 24 V, CLK F_{SW} = 1 MHz and $V_{EN/UVLO}$=2.5 V unless otherwise stated.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$VCC_{OVLO-FALLING}$	Input Over-voltage Lockout Falling Threshold	VCC falling	36.5	38.2	40.0	V	
$VCC_{OVLO-HYS}$	Input Over-voltage Lockout Hysteresis	VCC hysteresis voltage	0.47	0.57		V	
THERMAL SHUT DOWN							
T_{SD+}	T_{SD} turn on temperature	T_J rising	170	184	198	°C	
T_{SD-}	T_{SD} turn off temperature	T_J falling	135	147	159	°C	
$T_{SD-HYST}$	T_{SD} hysteresis		32	37	42	°C	

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7 Parameter Measurement Information

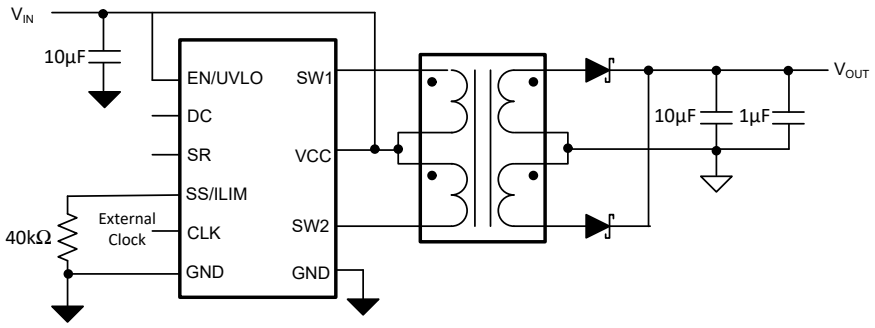

Figure 7-1. Measurement Circuit for Output

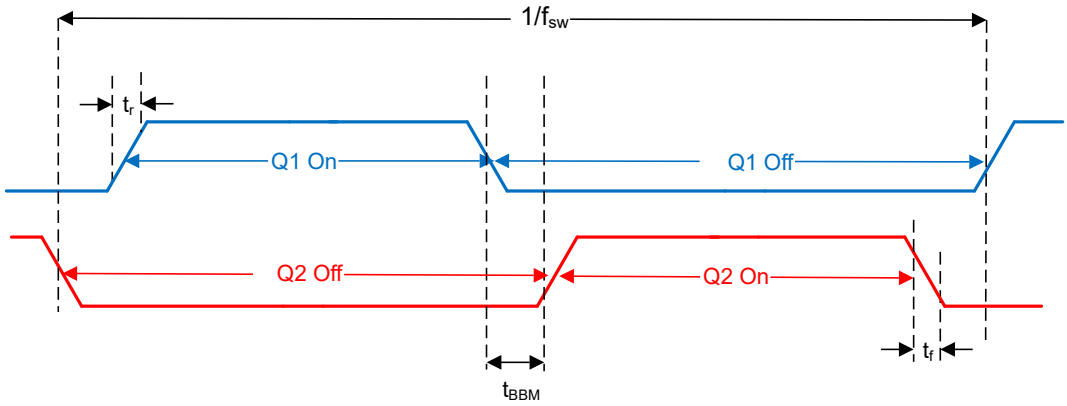

Figure 7-2. Timing Diagram

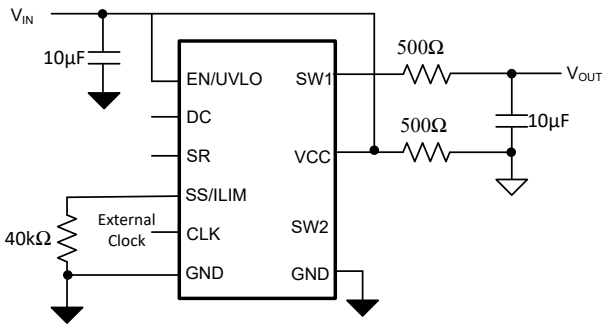

Figure 7-3. Test Circuit for $V_{(slew)}$

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8 Detailed Description

8.1 Overview

The SN6507 is a 36-V, 0.5-A push-pull transformer driver with two integrated n-channel power MOSFETs. It is designed for low cost, small size, low EMI isolated DC/DC power supplies.

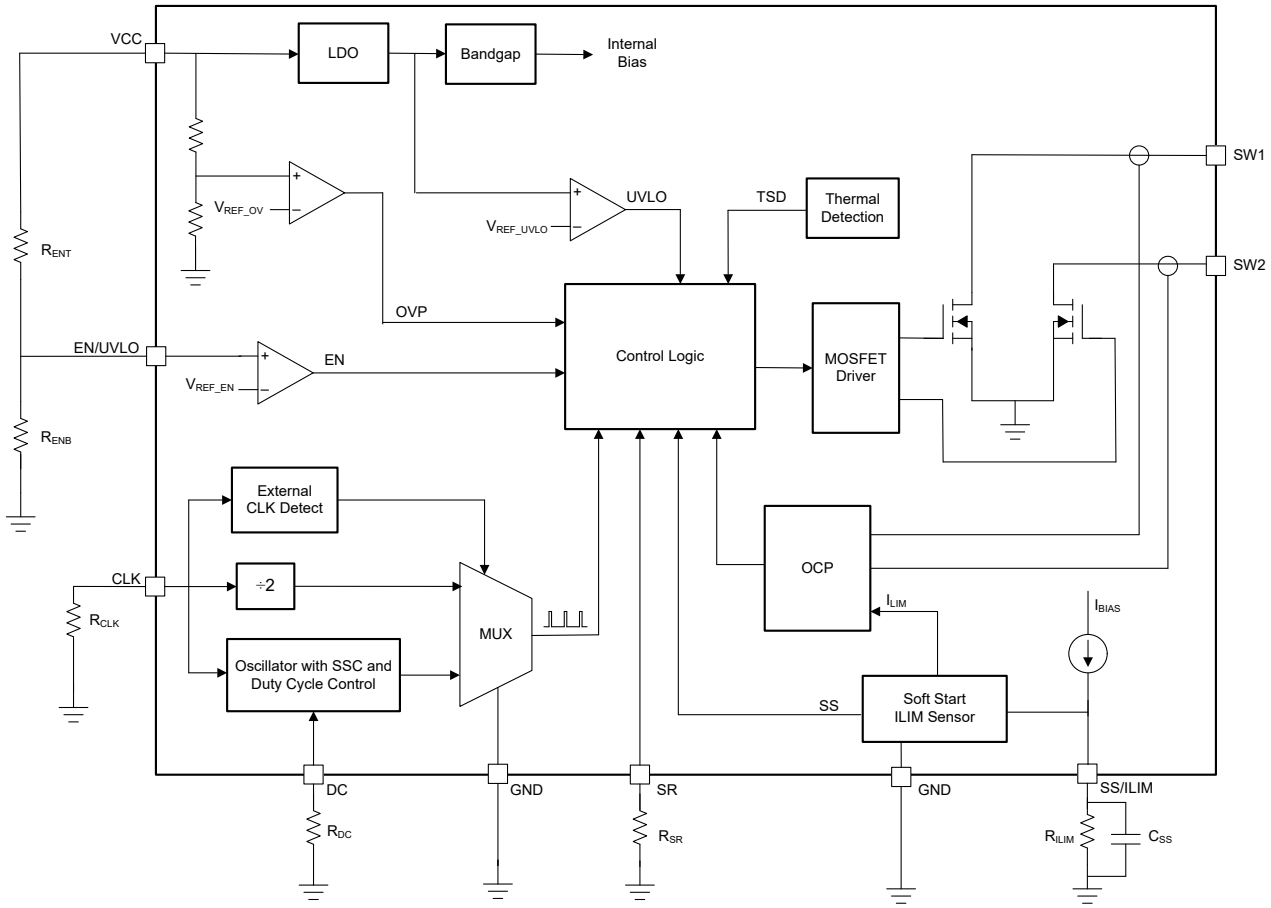
The device includes an oscillator that feeds a gate-drive circuit. The gate-drive, comprising a frequency divider and a break-before-make (BBM) logic, provides two complementary output signals which alternately turn the two output NMOS transistors on and off. A subsequent break-before-make logic inserts a dead-time between the high-pulses of the two signals, to avoid shorting out both ends of the transformer's primary windings. The resulting output signals, drive an isolation transformer and a rectifier, converting the input voltage to an isolated output voltage.

To improve performance at wide-input applications, the device implements a Duty Cycle Control (DCC) feature that the duty cyle is dynamically adjusted to compensate for the input variation. It removes the need of pre-regulation if the input variation is within a certain degree. Or even if at wide input conditions where the input variation is out of regulation range, it saves secondary-side LDO size and power loss. The wide switching frequency of 150 kHz to 2 MHz allows for better efficiency and smaller output ripple, as well as size optimization when selecting the transformers.

The transformer driver comes with multiple protection features to ensure robust operation, such as programmable overcurrent protection (OCP), input OVP, input UVLO and TSD. The device minimizes excessive output overvoltage transients by taking advantage of the overvoltage comparator. When the overvoltage comparator is activated, the MOSFETs are turned off and prevented from turning on until the overvoltage condition is removed. The device implements overload protection for both MOSFETs which help control the transformer current and avoid transformer saturation. It also shuts down if the junction temperature is higher than the thermal shutdown trip point. A programmable soft-start period reduces the inrush current during start-up and fault recovery.

For ultra-low EMI applications, the slew rate control feature provides design flexibility and simplicity to further improve emissions with a resistor-programmable option.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Push-Pull Converter

Push-pull converters require transformers with center-taps to transfer power from the primary to the secondary. When Q_1 conducts, V_{IN} drives a current through the lower half of the primary to ground, thus creating a negative voltage potential at the lower primary end with regards to the V_{IN} potential at the center-tap.

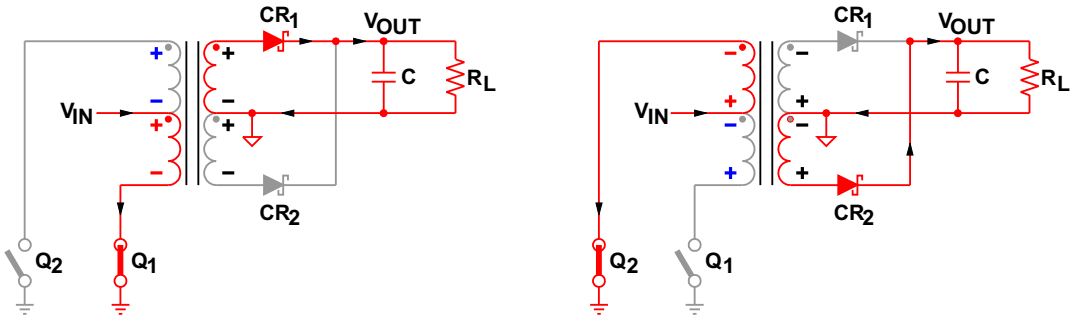


Figure 8-1. Switching Cycles of a Push-Pull Converter

At the same time the voltage across the upper half of the primary is such that the upper primary end is positive with regards to the center-tap in order to maintain the previously established current flow through Q_2, which now has turned high-impedance. The two voltage sources, each of which equaling V_{IN}, appear in series and cause a voltage potential at the open end of the primary of $2 \times V_{IN}$ with regards to ground.

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Per dot convention the same voltage polarities that occur at the primary also occur at the secondary. The positive potential of the upper secondary end therefore forward biases diode CR_1. The secondary current starting from the upper secondary end flows through CR_1, charges capacitor C, and returns through the load impedance R_L back to the center-tap.

When Q_2 conducts, Q_1 goes high-impedance and the voltage polarities at the primary and secondary reverse. Now the lower end of the primary presents the open end with a $2\times V_{IN}$ potential against ground. In this case CR_2 is forward biased while CR_1 is reverse biased and current flows from the lower secondary end through CR_2, charging the capacitor and returning through the load to the center-tap.

8.3.2 Core Magnetization

Figure 8-2 shows the ideal magnetizing curve for a push-pull converter with B as the magnetic flux density and H as the magnetic field strength. When Q_1 conducts the magnetic flux is pushed from A to A', and when Q_2 conducts the flux is pulled back from A' to A. The difference in flux and thus in flux density is proportional to the product of the primary voltage, V_P, and the time, t_{ON}, it is applied to the primary: $B \approx V_P \times t_{ON}$.

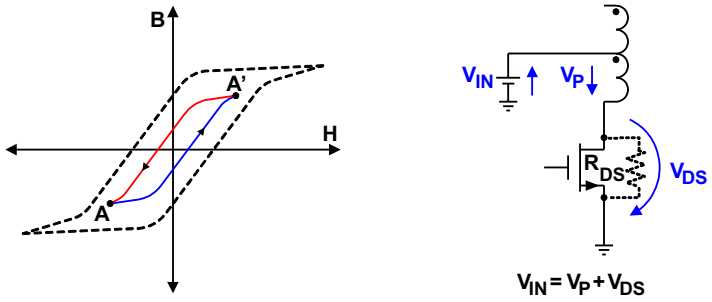

Figure 8-2. Core Magnetization and Self-Regulation Through Positive Temperature Coefficient of $R_{DS(on)}$

This volt-seconds (V-t) product is important as it determines the core magnetization during each switching cycle. If the V-t products of both phases are not identical, an imbalance in flux density swing results with an offset from the origin of the B-H curve. If balance is not restored, the offset increases with each following cycle and the transformer slowly creeps toward the saturation region.

Fortunately, due to the positive temperature coefficient of a MOSFET's on-resistance, the output FETs of the SN6507 have a self-correcting effect on V-t imbalance. In the case of a slightly longer on-time, the prolonged current flow through a FET gradually heats the transistor which leads to an increase in $R_{DS\text{-}on}$. The higher resistance then causes the drain-source voltage, VDS, to rise. Because the voltage at the primary is the difference between the constant input voltage, V_{IN}, and the voltage drop across the MOSFET, $V_P = V_{IN} - V_{DS}$, $V_P$is gradually reduced and V-t balance restored.

8.3.3 Duty Cycle Control

The SN6507 implements a duty cycle control feature to provide line regulation to a certain degree through a resistor on DC pin. By making the DC pin voltage a function of the input, the duty cycle will adjust with V_{IN}, so that V_{OUT} can be kept constant. Compared to fixed duty cycle transformer drivers, this dynamic duty cycle control feature reduces LDO power loss for wide V_{IN} variations by pseudo-regulating the output. For applications where input variation is within a certain range, this feature can eliminate the post-regulation LDO. Another benefit of duty cycle control is to reduce the transformer cost and size because of the limited input range to primary side of the transformer.

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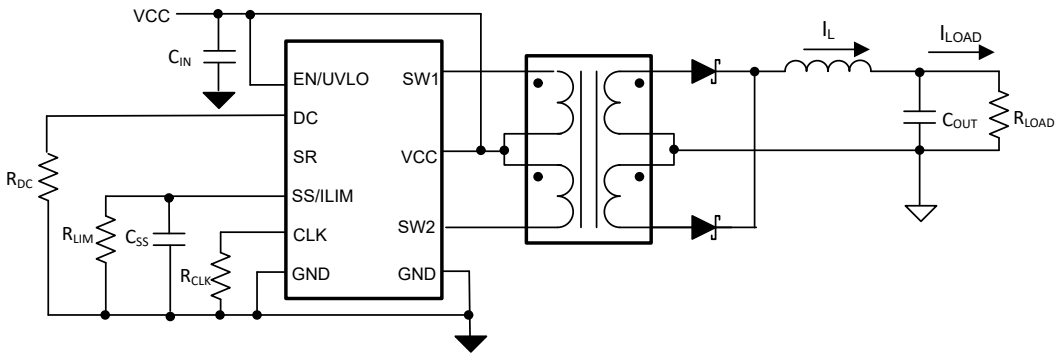

Figure 8-3. Schematic with duty cycle control

The calculation of DC pin resistor is shown in Equation 1, where both R_{DC} and R_{CLK} are in kΩ.

$$R_{DC} = 0.816 \times D \times VCC \times (R_{CLK} + 1\text{k}) - 1\text{k} \quad (1)$$

The duty cycle control can compensate for input variation up to ±35%, where line regulation within ±5% can be achieved. To achieve this range, it is recommended that duty cycle at nominal V_{IN} is centered at 25% (D = 0.25). The transformer turns ratio needs take this duty cycle into calculation, to ensure the expected output voltage level at all V_{IN} voltages, as discussed in Section 9.2.2.5.

The duty cycle control features supports up to a certain duty cycle and V_{IN} range. The minimum duty cycle is determined by the charge and discharge time of the gate capacitance of Power FETs, while the maximum duty cycle is limtied by the dead time (70 ns typical). For example, at 1 MHz, the adjustable duty cycle is between 10% and 43%. Exceeding above duty cycle range, the line regulation may saturate and input compensation does not work anymore. Meanwhile, if the duty cycle is lower than the minimum spec, the part may hit current limit at heavy loads. The V_{IN} range that duty cycle feature is applicable is from 6 V to 36 V.

To enable the duty cycle control feature, an inductor is required on the output side. The selection of the output inductor should make sure the inductor current will not go into discountinous conduction mode (DCM), meaning the inductor current ramp should not drop to zero at any time. The minimum inductance L_{MIN} is therefore calculated by the conditions that the part stays in continuous conduction mode (CCM) where the load DC current is smaller than half the current ramp amplitude seen on the inductor. Therefore L_{MIN} is a function of the load current and switching frequency as shown by below equation.

$$L_{MIN} = \frac{V_{OUT} T_{OFF}}{2 I_{LOAD}} = \frac{V_{OUT}}{2 I_{LOAD} f_{SW} (1 - D)} \quad (2)$$

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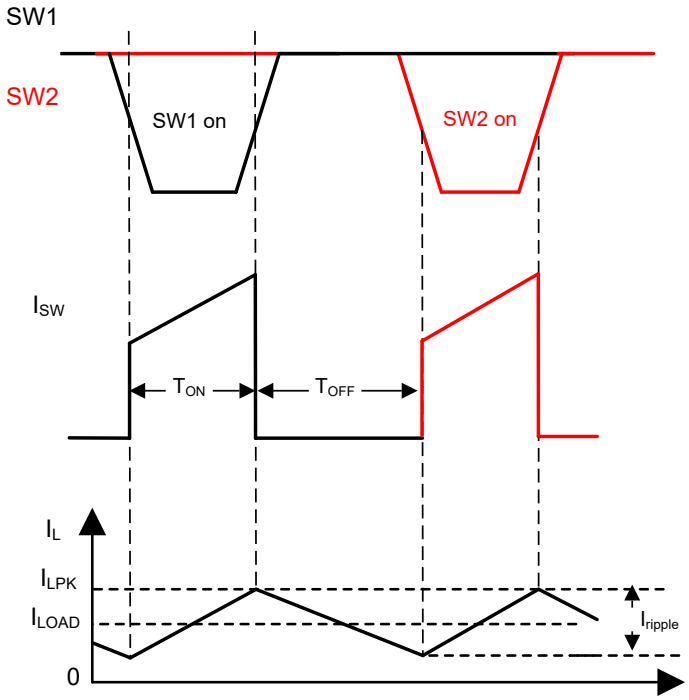

Figure 8-4. Waveforms in Continuous Conduction Mode (CCM)

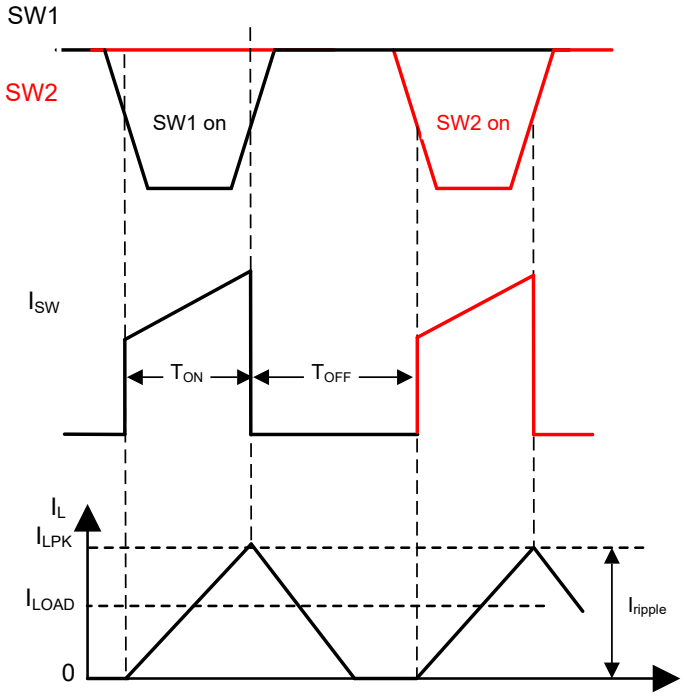

Figure 8-5. Waveforms in Discontinuous conduction Mode (DCM)

Programmable Switching Frequency

SN6507 has an internal oscillator to set the switching frequency of the power stage. As the two power switches are out of phase, the oscillator frequency is twice of the actual switching frequency of each power switch. The

duty cycle is fixed with 70 ns deadtime to avoid shoot-through. The duty cycle is changeable if duty cycle feature is enabled. Please refer to Section 8.3.4.

SN6507 has a wide switching frequency range from 150 kHz up to 2 MHz, which is pin programmable through a resistor (R_{CLK}) to GND. Below table lists the value of R_{CLK} to achieve certain operating frequencies (f_{SW}). The choice of switching frequency is a trade-off between power efficiency and size of capacitive and inductive components. For example, when operating at higher switching frequency, the size of the transformer and inductor is reduced, resulting in a smaller design footprint and lower cost. However, higher frequency increases switching losses and consequently degrades the overall power supply efficiency.

Table 8-1. Recommended 1% R_{CLK} values and f_{SW} Look-up Table

R_{CLK}	f_{SW} (Typical)
21 kΩ	500 kHz
9.6 kΩ	1 MHz
6.8 kΩ	1.5 MHz
4.1 kΩ	2 MHz
0 kΩ (Short to GND)	Default (1 MHz)

If CLK pin is shorted to GND, the part switches at its default frequency (1 MHz typical). CLK pin floating is taken as a fault condition and the part will stop switching.

8.3.4 Spread Spectrum Clocking

Radiated emissions is an important concern in high current switching power supplies. Due to the periodicity of the digital clock signals, the energy concentrates in one particular frequency and also in its odds harmonics, causing EMI issues. SN6507 implements Spread spectrum clocking (SSC) to reduce the radiated emissions of digital clock signals. The device modulates its internal clock in such a way that the emitting energy is spread over multiple frequency bins. This feature greatly improves the emissions performance of the entire power supply block and hence relieves the system designer from one major concern in isolated power supply design.

8.3.5 Slew Rate Control

To allow optimization of EMI with respect to efficiency, the SN6507 is designed to allow a resistor (R_{SR}) to select the strength of the driver of PowerFETs turning on. As shown in Figure 8-6 below, the slew rate of the switching edges is controllable with the resistor. Rolling off harmonics through slew rate control can eliminate the need for shielding and common mode chokes in many applications.

The EMI benefit of slew rate control may result in slightly reduced efficiency and higher peak current (I_{SW_SR}). When the feature slows down the charging and discharging of the gate capacitance, the extended transition times of the FETs increases the transition losses during each switching cycle. This increases power dissipation, which decreases efficiency and exacerbates thermal concerns. This will limit how much the slew rate can be reduced. Another cost is the peak current of each cyle will be increased. It is because the slow edges reduce the on-time (I_{ON_SR}) and eventually the peak current (I_{SW_SR}) will increase to deliver the same average current to the load on each cycle.

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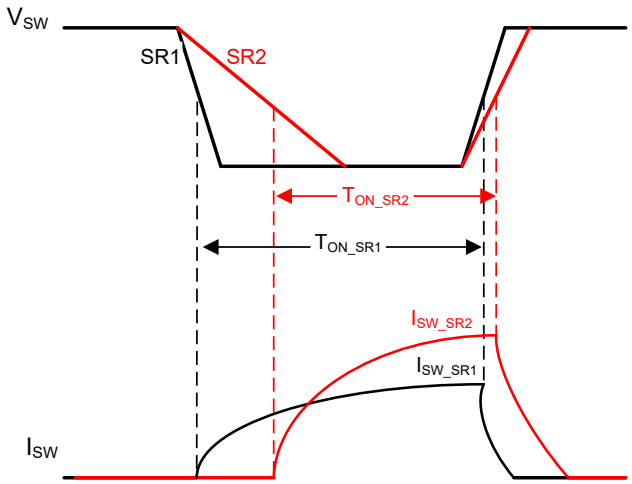

Figure 8-6. Slew Rate Control Scheme

The slew rate at different V_{IN} is programmed by R_{SR}. The relationship between V_{IN} and the slew rate are listed in Table 8-2 below. As the slew rate is independent of the switching frequency, care must be taken that at high frequencies, the slew rate should be fast enough to maximize the output power delivery to the load. If the SR pin ijs left floating, the slew rate will be set to the default value. SR pin short to GND is taken as a fault condition and the device will stop switching.

Table 8-2. Slew Rate Control Look-up Table

VCC (V)	R_{SR} (kΩ)	Typical SLEW RATE (V/µs)
5	4.8	337
5	Floating (Default)	263
5	15	224
5	21	198
12	4.8	424
12	Floating (Default)	298
12	15	237
12	21	199
24	4.8	583
24	Floating (Default)	369
24	15	273
24	21	218
36	4.8	646
36	Floating (Default)	406
36	15	298
36	21	237

8.3.6 Protection Features

SN6507 is protected by multiple protection features to improve the system level robustness and reliability. The protection features include programmable input undervoltage protection (UVLO), input over-voltage protection (OVP), programmable over current protection (OCP), and over-temperature protection (TSD).

8.3.6.1 Over Voltage Protection (OVP)

As SN6507 is a open-loop transformer driver, the over voltage protection feature is implemented to prevent the output voltage from rising too high. The overvoltage protection threshold is a fixed value and cannot be programmed. If the VCC pin voltage exceeds the overvoltage rising threshold, device stops switching after a 550

ns (typical) response time. To recover from an over voltage event, the input voltage must drop below the OVP falling threshold.

8.3.6.2 Over Current and Short Circuit Protection

The SN6507 is protected from overcurrent conditions with cycle-by-cycle current limiting on both NMOS switches. The switch current is sensed and compared to the current threshold that is programmed by the external resistor on SS/ILIM pin. OCP protection is disabled during soft-start. After soft-start finishes, the OCP is enabled and the threshold is set at the programmed value. The recommended resistor (R_{ILIM}) and its relationship with current limit threshold (I_{LIM}) is listed in Table 8-3 below. Leaving the ILIM/SS pin floating is not recommended for this device.

Table 8-3. Recommended 1% R_{ILIM} values

R_{ILIM}	I_{LIM} (Typical)
18 kΩ	1.3 A
20 kΩ	1.2 A
22 kΩ	1.1 A
24 kΩ	1.0 A
27 kΩ	900 mA
30 kΩ	800 mA
35 kΩ	700 mA
40 kΩ	600 mA
50 kΩ	500 mA
62 kΩ	400 mA
85 kΩ	300 mA
127 kΩ	200 mA
261 kΩ	100 mA

In case of an extreme over-load condition on the isolated output due to short circuit, the device behaves as follows:

- In the event of an overload or transient short, if the voltage dip is lower than 2.5 V (typical),the device considers it as a “soft-short” condition. At soft-short, the converter goes to hiccup mode. On hitting the programmed OCP threshold, the driver will be shut-off for 100 ns (typical) and then retry driving. If the OCP trips again, the cycle continues. This retry keeps on happening for entire T_{ON} time of SW1 and SW2 till OCP does not trip or hard fault gets triggered. During the OCP retry events, both FET are turned off and the transient peak current may go higher than OCP limit.
- If the voltage dip is more than 2.5 V (typical), the devices considers it as a “hard-short” condition. The hard-short OCP threshold is fixed at 5 A (typical). If hard-short condition lasts more than 200 µs, it indicates that the system is in a serious short-circuit fault condition, the device will fully discharge the soft-start cap and enters soft start. Note there is a 65 ns response time to trigger hard-short OCP.

8.3.6.3 Under Voltage Lock-Out (UVLO)

Start-up and shutdown are controlled by the both EN/UVLO pin and VCC pin. For the device to remain in shutdown mode, apply a voltage below EN_{UVLO} to the EN/UVLO pin. In shutdown mode, the quiescent current is less than 0.8 µA (typical). If EN/UVLO pin sees a voltage higher than EN_{UVLO}, but V_{IN} is still below VCC_{UVLO}, the SW node is inactive. Once the V_{IN} is above VCC_{UVLO}, the chip begins to switch normally, provided the EN/UVLO voltage is above 1.5 V.

There are three ways to enable the device operation. The simplest way is to connect the EN/UVLO pin to VCC pin, allowing self-start-up of the device when VCC pin voltage is above VCC_{UVLO} level. However, many applications benefit from an input UVLO level different than that provided internal UVLO. So another way is to employ an enable resistor divider network as shown in Figure below, which establishes a programmable UVLO threshold. The thrid way is to connect an external logic output to drive this pin, allowing user-defined system power sequencing.

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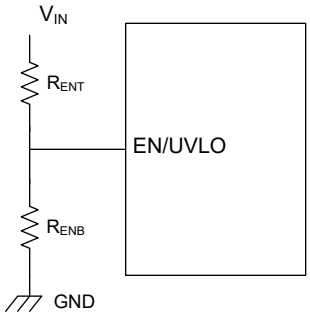
EN/UVLO pin has a 5 µs (typical) glitch filter to help avoid false turn-on and turn-off due to noise coupling. It also comes with an internal pull down design to ensure the device is in shutdown mode when the pin is left floating.

Programmable UVLO using EN/UVLO pin



Resistor values can be calculated using Equation below, where the input turn on threshold V_{IN_UVLO} is the desired typical start-up input voltage and EN_{UVLO} is 1.5 V typical.

$$V_{IN\_UVLO} = \left(1 + \frac{R_{ENT}}{R_{ENB}}\right) \times EN_{UVLO} \quad (3)$$

8.3.6.4 Thermal Shut Down (TSD)

Thermal shutdown prevents the device from reaching extreme junction temperatures by turning off the internal switches when the IC junction temperature exceeds 180°C (typical). In TSD, the switching stops immediately to prevent the internal MOSFETs from failing in either high ambient temperature operation conditions or due to self-heating from high switching current. To recover from thermal shut down condition, the junction temperature must be below the overtemperature protection falling threshold. When the junction temperature falls below 147°C (typical), the power FET switching is enabled.

8.4 Device Functional Modes

The functional modes of the device are divided into start-up, operating, and off-mode.

8.4.1 Start-Up Mode

When VCC pin voltage ramps up to VCC_{UVLO} , and EN/UVLO pin voltage is over EN_{UVLO} the internal oscillator starts operating. The output stage begins switching but the amplitude of the drain signals at SW1 and SW2 have not reached its full maximum yet.

8.4.1.1 Soft-Start

SN6507 device supports soft-start feature. Upon power up or when EN/UVLO pin transitions from Low to High, the gate drive of the output powerFET is gradually increased over a period of time from 0 V to full driving strength. Soft-start prevents high inrush current from VCC while charging large secondary side decoupling capacitors, and also prevents overshoot in secondary voltage during power-up.

The sort-start time to ramp to the peak switch current is calculated by the capacitor and resistor on SS/ILIM pin with the following formula.

$$T_{SS} = \frac{C_{SS}}{275\mu A - \frac{0.6}{R_{ILIM}}} \quad (4)$$

During soft-start, the over-current protection is disabled. To esnsure a smooth transition between soft-start and the steady state, it's recommended to have a minimum of 50 nF C_{SS} and output capacitor C_{OUT} is at less than 10 times of C_{SS}.

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8.4.2 Operation Mode

The SN6507 driver is in operation mode when EN pin is above EN_{UVLO}, VIN pin is above VCC_{UVLO}, and soft-start completes. In normal operation mode, the switching frequency is fixed, determined either by the CLK pin resistor or external Clock signal.

8.4.3 Shutdown Mode

The device has a dedicated EN/UVLO pin to put the device in very low power mode to save power when not in use. EN/UVLO pin has an internal pull down resistor which keeps device disabled when not driven. When disabled or when V_{CC} is < 2.8 V , both drain outputs, SW1 and SW2, are tri-stated.

8.4.4 SYNC Mode

The SN6507 has a CLK pin which can be used to synchronize the device with system clock and in turn with other SN6507 devices so that the system can control the exact switching frequency of the device. In SYNC mode, the CLK frequency is divided by two to drive the gates of powerFETs. Figure 9-2 shows the timing diagram for the same.

The device can automatically changes from SYNC mode to the internal or resistor CLK mode, if a valid external clock is not present for a certain period of time ($t_{CLKTIMER}$). Similarly, when the part transitions from internal or resistor controlled CLK mode to SYNC mode, there will be five CLK cycles delay for external CLK detection.

When the device is in SYNC mode, duty cycle control and SSM are not supported., therefore it's recommended to leave DC pin floating in SYNC mode for reduce the solution size.

Note that it's recommended that VCC pin powers up before CLK pin. Otherwise the initial state of external clock should be high-Z.

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN6507 is a transformer driver designed for low-cost, small form-factor, isolated DC/DC converters using the push-pull topology. The device includes an oscillator that feeds a gate-drive circuit. The gate-drive, comprising a frequency divider and a break-before-make (BBM) logic, provides two complementary output signals which alternately turn the two output transistors on and off.

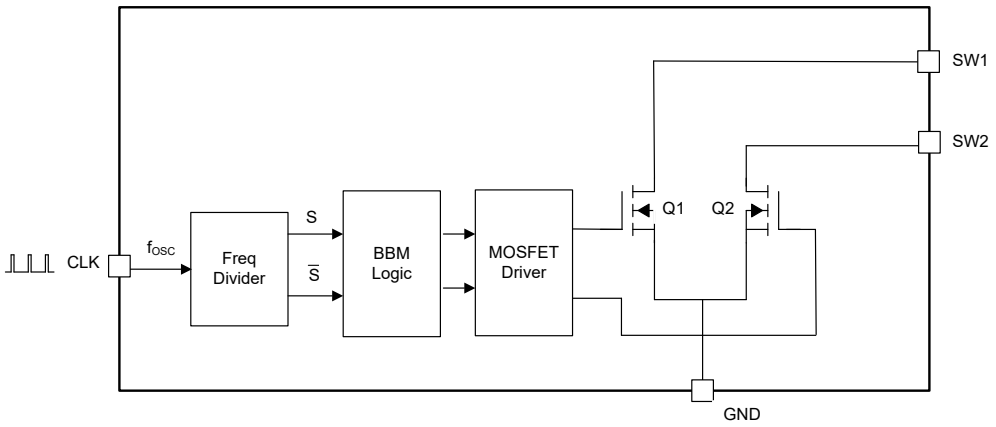

Figure 9-1. Block Diagram With Break-Before-Make Action

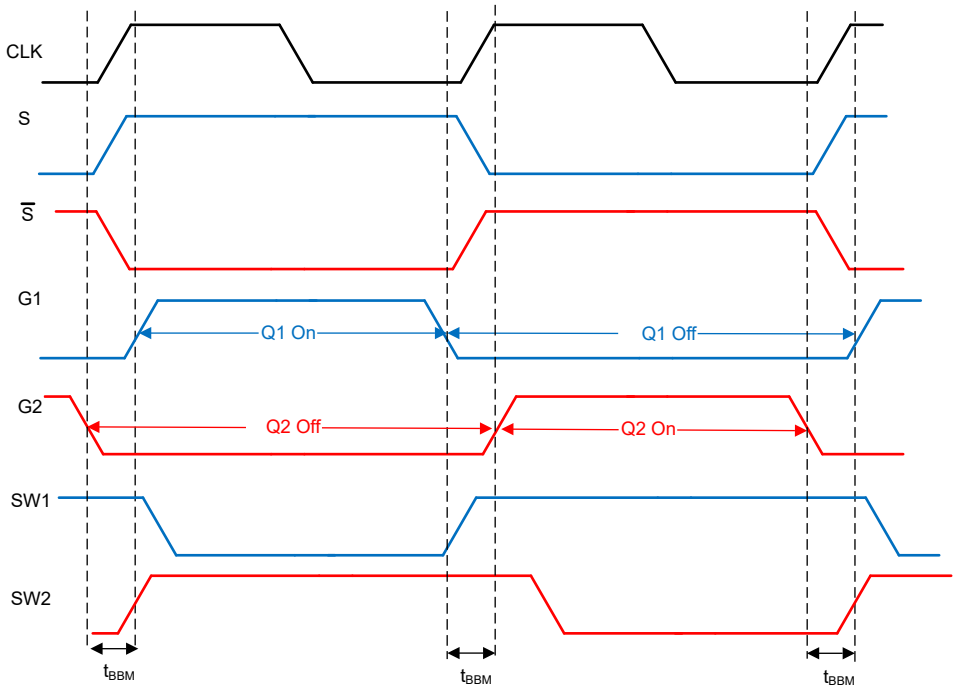

Figure 9-2. Output timing with Break-Before-Make Action

The output frequency of the oscillator is divided down by an asynchronous divider that provides two complementary output signals, S and $\overline{S}$, with a 50% duty cycle. A subsequent break-before-make logic inserts a dead-time between the high-pulses of the two signals. The resulting output signals, G_1 and G_2, present the gate-drive signals for the output transistors Q_1 and Q_2. As shown in Figure 9-2, before either one of the gates can assume logic high, there must be a short time period during which both signals are low and both transistors are high-impedance. This short period, known as break-before-make time, is required to avoid shorting out both ends of the primary.

9.2 Typical Application

Two application cases are discussed. One is for Fixed input with slew rate control. The other is for wide-ranging input with duty cycle control.

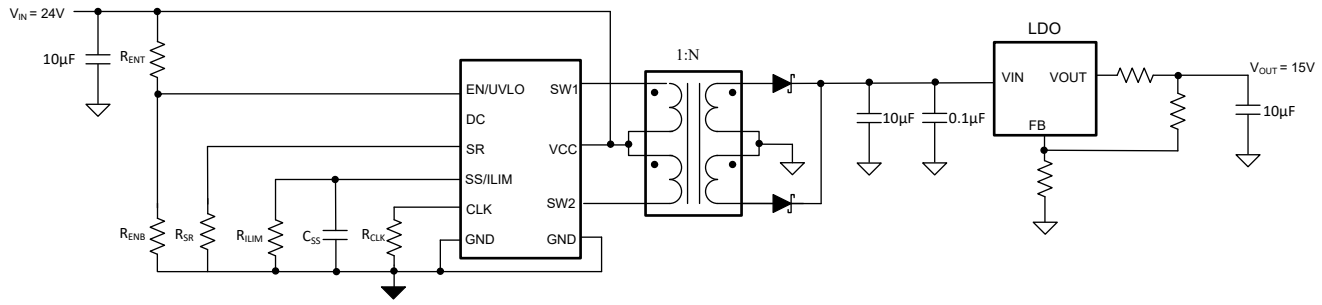

Figure 9-3. Typical Application Schematic for Fixed Input with Slew Rate Control

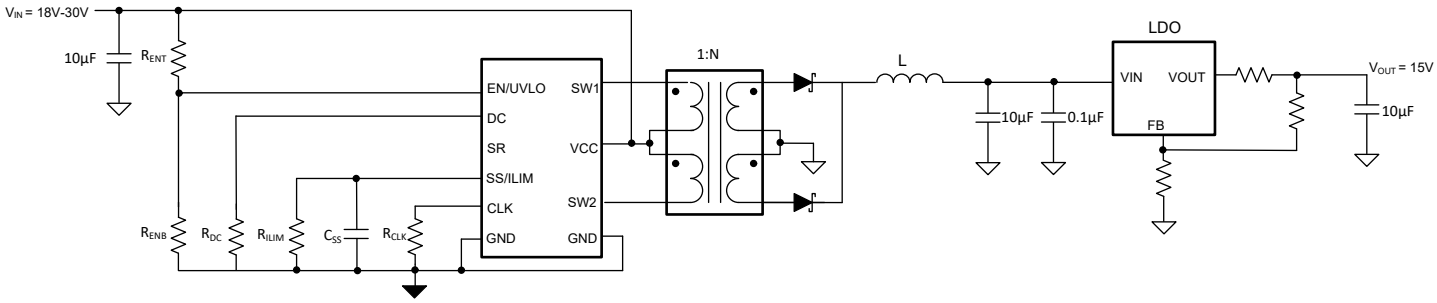

Figure 9-4. Typical Application Schematic for Wide-Ranging Input with Duty Cycle Control

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 9-1 as design parameters.

Table 9-1. Design Parameters

PARAMETER	COMMENT	EXAMPLE VALUE
Fixed V_{IN}	Input voltage for fixed input case	24 V ± 2%
Wide-ranging V_{IN}	Input voltage range for wide-input case	18 V (min) 24 V (typ.) 30 V (max)
f_{SW}	Switching frequency	1 MHz ± 10%
V_{OUT}	Output voltage	15 V
I_{LOAD}	Load current	200 mA
I_{LIM}	Peak Current Limit	500 mA
UVLO	Under Voltage Lockout	9 V
SS	Soft-Start Time	2 ms

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9.2.2 Detailed Design Procedure

This section presents a detailed design procedures using SN6507 transforme driver. The following recommendations on components selection focus on the design of an efficient push-pull converter with high current drive capability. Two cases are discussed: wide input range with duty cycle control, and a compact design with a fixed input voltage.

The pin configuration of SN6507 are discussed by 5 simple steps, followed by the selection of external components, including diodes, capacitors, inductor, LDO and transformers.

9.2.2.1 Pin Configuration

Here is an example of how to configure the SN6507 pins in 5 simple steps.

Step 1: Set the Switching Frequency

First, set the driver switching frequency with R_{CLK} using Table 8-1.

For example: R_{CLK} = 9.6 kΩ or shorted to GND, sets typical f_{SW} at about 1 MHz.

Step 2: Set the Input UVLO

The EN/UVLO (undervoltage lockout) pins are used to set minimum input voltage that the driver starts switching. The resister divider value can be calculated by Equation 3.

For example, if the input threshold (V_{ON}) is expected to be at 9 V, the resistors are calculated as R_{ENT}/R_{ENB} = 5

Therefore,the resistors values are chosen as:

R_{ENT}= 5 kΩ, R_{ENB}= 1 kΩ

To make the device self-start at default UVLO thresold (2.8 V typical), users can skip Step 2 and directly short the EN/UVLO pin to VCC.

Step 3: Set the Current Limit and Soft-Start Time

The curren limit can be set by a resistor on SS/ILIM pin according to Table 8-3.

For example, to set the current limit is set at 500 mA (typical), the recommended R_{ILIM} is 50 kΩ.

Once R_{ILIM} is determined, substitue R_{ILIM} into Equation (4), the soft-time calculation is:

$$T_{SS} = \frac{C_{SS}}{275\mu A - \frac{0.6}{50\text{k}}}$$

Taking 2 ms (typical) soft-start time as an example, the capacitor on SS/ILIM pin :C_{SS} = 0.5 uF.

Note that both R_{ILIM} and C_{SS} are required on SS/ILIM pin to ensure the robust operation of this device. Missing the RC connection or leaving the pin floating should be avoided.

Step 4: Set the Duty Cycle

For fixed input cases, the duty cycle feature is not needed. This step can be skipped by leaving DC pin floating, so that the part will operate at default maximum duty (48% typical). The maximum duty cycle is determined by the switching period and the deadtime (70 ns typical) to avoid overlap of two power switches.

For wide-input cases, the duty cycle feature can be enabled by connecting a resistor R_{DC} on DC pin, and an inductor at the output side. The inductor selection is presented in Section 9.2.2.4.

To achieve maximum input compensation, the DC is set close to 0.25 (25% duty cycle) at typical VCC (24 V). The R_{DC} is calculated as 240 kΩ by substituting DC = 0.25, VCC = 24 V, and R_{ILIM} = 50 into the equation below, where both R_{ILIM} and R_{DC} are in kΩ.

$$R_{DC} = 0.816 \times DC \times VCC \times (R_{ILIM} + 1) - 1$$

9.2.2.2 LDO Selection

SN6507 is an open-loop transformer driver without load regulation capability. The output voltage may vary over a wide range load current. Therefore, if a high-accuracy, load independent supply is required, the implementation of a low dropout regulator (LDO) on the output side is strongly advised.

The minimum requirements for a suitable low dropout regulator are:

- Its current drive capability should slightly exceed the specified load current of the application to prevent the LDO from dropping out of regulation. Therefore, for a load current of 200 mA, choose a 200 mA to 300 mA LDO. While regulators with higher drive capabilities are acceptable, they also usually possess higher dropout voltages that will reduce overall converter efficiency.
- The internal dropout voltage, V_{DO}, at the specified load current should be as low as possible to maintain efficiency. For a low-cost 300 mA LDO, a V_{DO} of 600 mV at 300 mA is common. Be aware; however, that this lower value is usually specified at room temperature and can increase by a factor of 2 over temperature, which in turn will raise the required minimum input voltage.
- The required minimum input voltage preventing the regulator from dropping out of line regulation is given with:

$$V_{I\text{-}min} = V_{DO\text{-}max} + V_{O\text{-}max} \quad (5)$$

  This means in order to determine V_I for worst-case condition, the user must take the maximum values for V_{DO} and V_O specified in the LDO data sheet for rated output current (that is, 200 mA) and add them together. Also specify that the output voltage of the push-pull rectifier at the specified load current is equal or higher than $V_{I\text{-}min}$. If it is not, the LDO will lose line-regulation and any variations at the input passes straight through to the output. Hence, below $V_{I\text{-}min}$ the output voltage follows the input and the regulator behaves like a simple conductor.
- The maximum regulator input voltage must be higher than the rectifier output under no-load. Under this condition there is no secondary current reflected back to the primary, thus making the voltage drop across $R_{DS\text{-}on}$ negligible and allowing the entire converter input voltage to drop across the primary. At this point, the secondary reaches its maximum voltage of

$$V_{S\text{-}max} = V_{IN\text{-}max} \times N \quad (6)$$

with $V_{IN\text{-}max}$ as the maximum converter input voltage and n as the transformer turns ratio. Thus to prevent the LDO from damage the maximum regulator input voltage must be higher than $V_{S\text{-}max}$. Table 9-2 lists the maximum secondary voltages for various turns ratios commonly applied in push-pull converters.

Table 9-2. Required Maximum LDO Input Voltages for Various Push-Pull Configurations

PUSH-PULL CONVERTER				LDO
CONFIGURATION	$V_{IN\text{-}max}$ [V]	TURNS-RATIO (N)	$V_{S\text{-}max}$ [V]	$V_{I\text{-}max}$ [V]
24 V_{IN} to 15 V_{OUT}	25	1.38:1	18	25
12 V_{IN} to 15 V_{OUT}	12.5	1:1.5	19	25

9.2.2.3 Diode Selection

A rectifier diode should always possess low-forward voltage to provide as much voltage to the converter output as possible. However, when SN6507 is used in high-frequency switching applications, the diode must also possess a low total capacitance, a short recovery time and a current rating greater than the load current. Schottky diodes meet these requirements and are therefore strongly recommended in SN6507 push-pull converter designs. .

The diode voltage rating is determined by the transformer secondary side voltage plus any voltage ringing. The voltage ringing, however, is difficult to predict, because it depends on multi factors, such as loop resistance, the leakage inductance of the transformer, and the diode junction capacitance. As a rule of thumb, the diode voltage rating should be at least 1.5 times the transformer turns ratio multiplied by the maximum input voltage. Because the two secondary windings are connected across the rectifier bridge, a factor of two is needed, producing the diode maximum DC blocking voltage rating:

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$$V_{DIODE} = 1.5 \times 2N \times V_{IN(MAX)} \quad (7)$$

For example, a good choice for 15 V output is PMEG200G20ELRX for optimized EMI performance.

9.2.2.4 Capacitor and Inductor Selection

Capacitor Selection

The capacitors in the push-pull converter circuits are normally multi-layer ceramic chip (MLCC) capacitors. As with all high speed CMOS ICs, the device requires a bypass capacitor in the range of 10 nF to 100 nF.

The input bulk capacitor at the center-tap of the primary supports large currents into the primary during the fast switching transients. For minimum ripple make this capacitor 1 µF to 10 µF. In a 2-layer PCB design with a dedicated ground plane, place this capacitor close to the primary center-tap to minimize trace inductance. In a 4-layer board design with low-inductance reference planes for ground and V_{IN}, the capacitor can be placed at the supply entrance of the board. To ensure low-inductance paths use two vias in parallel for each connection to a reference plane or to the primary center-tap.

The bulk capacitor at the rectifier output smooths the output voltage. Make this capacitor 1 µF to 10 µF.

The small capacitor at the regulator input is not necessarily required. However, good analog design practice suggests, using a small value of 47 nF to 100 nF improves the regulator's transient response and noise rejection.

The LDO output capacitor buffers the regulated output for the subsequent isolator and transceiver circuitry. The choice of output capacitor depends on the LDO stability requirements specified in the data sheet. However, in most cases, a low-ESR ceramic capacitor in the range of 4.7 µF to 10 µF will satisfy these requirements.

To avoid hitting OCP at the transistion from soft-start to steady state, the output capacitor C_{OUT} is recommended to be less than 10 times of C_{SS} on SS/ILIM pin. Otherwise, if there is a short soft-start time due to small C_{SS}, the output capacitor is only partially charged and sees high current spikes on first cycles after the device enters active mode.

Inductor Selection

The inductor is required only for duty cycle feature. The minimum inductor value (L_{MIN}) is set by the peak current limit of internal switcher (I_{LIM}) as calculated by Equation (2). Higher inductance produces better regulation and lower voltage ripple, but requires a correspondingly larger size inductor. The optimum inductor value is determined by taking into account the tradeoff between the regualtion performance and the size.

For example, when V_{OUT} = 15 V, f_{SW} = 1 MHz, D = 0.25, the minimum inductoance is calculated to be 50 µH.

$$L_{MIN} = \frac{15V}{2 \times 0.2A \times 1MHz \times (1 - 0.25)} = 50\mu H \quad (8)$$

9.2.2.5 Transformer Selection

9.2.2.5.1 V-t Product Calculation

To prevent a transformer from saturation its V-t product must be greater than the maximum V-t product applied by the device. The maximum time this voltage is applied to the primary is half the period of the lowest frequency at the specified input voltage. Therefore, the transformer's minimum V-t product is determined through:

$$Vt_{min} \geq V_{IN\text{-}max} \times \frac{T_{max}}{2} = \frac{V_{IN\text{-}max}}{2 \times f_{min}} \quad (9)$$

Example of Fixed Input:

Taking the assumption of $f_{SW(min)}$ as 0.9 MHz with a $V_{IN(max)}$ 24 V supply, Equation 9 yields the minimum V-t products of:

$$Vt_{min} \geq \frac{24V}{2 \times 0.9MHz} = 13\,V\mu s \quad (10)$$

Example of Wide-Ranging Input:

Taking the assumption of $f_{SW(min)}$ as 0.9 MHz with a $V_{IN(max)}$ 30 V supply, Equation 9 yields the minimum V-t products of:

$$Vt_{min} \geq \frac{30V}{2 \times 0.9MHz} = 16.7\ V\mu s \quad (11)$$

While Vt-wise all of these transformers can be driven by the device, other important factors such as isolation voltage, transformer wattage, and turns ratio must be considered before making the final decision.

9.2.2.5.2 Turns Ratio Estimate

From previous section, it has been determined that the transformer chosen must have a V-t product of 15 Vµs. However, before searching the manufacturer web sites for a suitable transformer, the user still needs to know its minimum turns ratio that allows the push-pull converter to operate flawlessly over the specified current and temperature range. This minimum transformation ratio is expressed through the ratio of minimum secondary to minimum primary voltage multiplied by a correction factor that takes the transformer's typical efficiency of 97% into account:

$$V_{P\text{-}min} = V_{IN\text{-}min} - V_{DS\text{-}max} \quad (12)$$

$V_{S\text{-}min}$ must be large enough to allow for a maximum voltage drop, $V_{F\text{-}max}$, across the rectifier diode and still provide sufficient input voltage for the regulator to remain in regulation. From the *Section 9.2.2.2* section, this minimum input voltage is known and by adding $V_{F\text{-}max}$ gives the minimum secondary voltage with:

$$V_{S\text{-}min} = V_{F\text{-}max} + V_{DO\text{-}max} + V_{O\text{-}max} \quad (13)$$

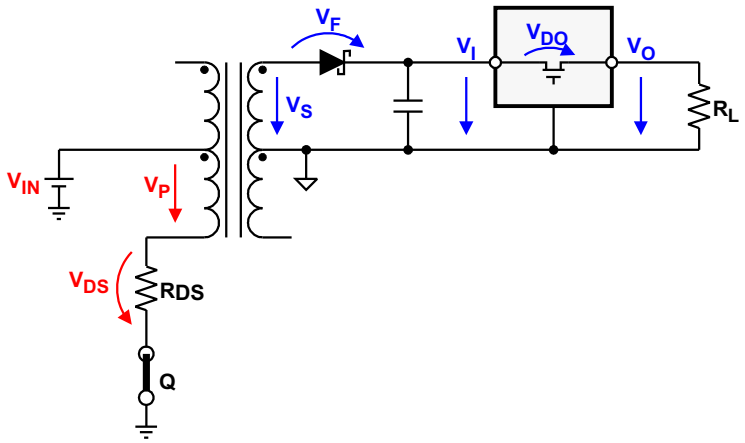

Figure 9-5. Establishing the Required Minimum Turns Ratio Through $N_{min} = 1.03 \times V_{S\text{-}min} / V_{P\text{-}min}$

Then calculating the available minimum primary voltage, $V_{P\text{-}min}$, involves subtracting the maximum possible drain-source voltage of the device, $V_{DS\text{-}max}$, from the minimum converter input voltage $V_{IN\text{-}min}$:

$$V_{P\text{-}min} = V_{IN\text{-}min} - V_{DS\text{-}max} \quad (14)$$

$V_{DS\text{-}max}$ however, is the product of the maximum $R_{DS(on)}$ and I_D values for a given supply specified in the data sheet:

$$V_{DS\text{-}max} = R_{DS\text{-}max} \times I_{Dmax} \quad (15)$$

Then inserting Equation 15 into Equation 14 yields:

$$V_{P\text{-}min} = V_{IN\text{-}min} - R_{DS\text{-}max} \times I_{Dmax} \quad (16)$$

and inserting Equation 16 and Equation 13 into Equation 12 provides the minimum turns ration with:

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$$N_{min} = 1.03 \times \frac{V_{F-max} + V_{DO-max} + V_{O-max}}{V_{IN-min} - R_{DS-max} \times I_{D-max}} \quad (17)$$

Examples are given on the calculation method. One is for the fixed input case without duty cycle control. Tthe other is for the wide-ranging input, with or without duty cycle control.

Example of Fixed Input:

For a fixed 24 V V_{IN} to 15 V_{OUT} converter using the rectifier diode PMEG200G20ELRX and the LM317A LDO, the data sheet values taken for a load current of 500mA and a maximum temperature of 85°C are V_{F-max} = 0.5 V, V_{DO-max} = 0.7 V, and V_{O-max} = 15.15 V.

Then assuming that the converter input voltage is taken from a 24V regulated supply with a maximum ±2% accuracy makes V_{IN-min} = 23.52 V. Finally the maximum values for drain-source resistance and drain current at 24 V are taken from the data sheet with R_{DS-max} = 1 Ω and I_{D-max} = 0.5 A.

Inserting the values above into the Equation above yields a minimum turns ratio of:

$$N_{min} = 1.03 \times \frac{0.5\,V + 0.7\,V + 15.1\,V}{23.52\,V - 1\,\Omega \times 0.5\,A} = 0.72 \quad (18)$$

Example of Wide-Ranging Input:

- **Wide-Ranging Input without Duty-Cycle Control**

For converter designs with wide-input range but no duty cycle control, the turns ratio needs to take the minium input voltage into consideration.

Assuming the same diode and LDO are used, the calculation, so V_{F-max} = 0.5 V, V_{DO-max} = 0.7 V, and V_{O-max} = 15.15 V.

The input range from 18 V up to 30 V makes V_{IN-min} = 18 V. The input range from 18 V up to 30 V with 24 V typical makes V_{IN-min} = 18 V. Substituting the same R_{DS-max} = 1 Ω and I_{D-max} = 0.5 A into the Equation above yields to a minimum turns ratio of:

$$N_{min} = 1.03 \times \frac{0.5\,V + 0.7\,V + 15.1\,V}{18\,V - 1\,\Omega \times 0.5\,A} = 0.96 \quad (19)$$

- **Wide-Ranging Input with Duty-Cycle Control**

For converter designs with wide-input range, the duty cycle feature is useful to compensate input variaton. But care must be taken to make sure that high turns ratios don’t lead to primary currents that exceed the specified current limits of the device.

$$N_{min} = 1.03 \times \frac{V_{F-max} + V_{DO-max} + V_{O-max}}{V_{IN-typ} - R_{DS-max} \times I_{D-max}} \times \frac{1}{2D_{typ}} \quad (20)$$

Assuming the same diode and LDO are used, so V_{F-max} = 0.5 V, V_{DO-max} = 0.7 V, and V_{O-max} = 15.15 V.

It's recommends the use to set the DC=25% at typical V_{IN-typ} = 24 V. Substituting the same R_{DS-max} = 1 Ω and I_{D-max} = 0.5 A into the Equation above yields to a minimum turns ratio of:

$$N_{min} = 1.03 \times \frac{0.5\,V + 0.7\,V + 15.1\,V}{24\,V - 1\,\Omega \times 0.5\,A} \times \frac{1}{2 \times 0.25} = 1.38 \quad (21)$$

ADVANCE INFORMATION

9.2.3 System Examples

9.2.3.1 Higher Output Voltage Designs

The device can drive push-pull converters that provide doubling output voltages, or bipolar outputs with different rectifier topologies . Figure 9-6 to Figure 9-8 show some of these topologies together with their respective open-circuit output voltages.

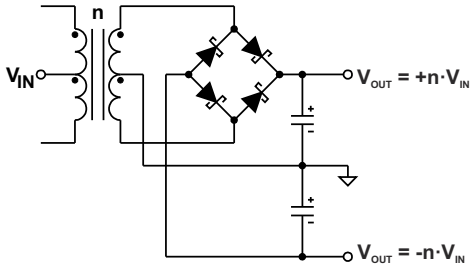


Figure 9-6. Bridge Rectifier With Center-Tapped Secondary Enables Bipolar Outputs

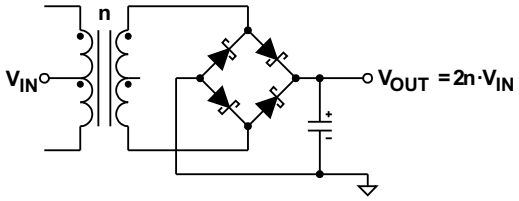


Figure 9-7. Bridge Rectifier Without Center-Tapped Secondary Performs Voltage Doubling

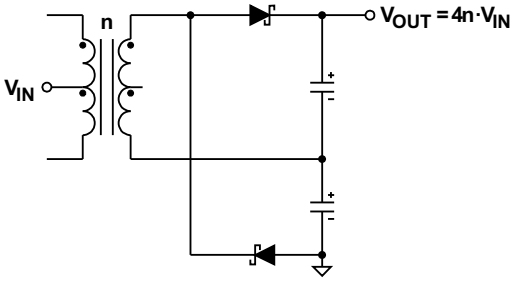


Figure 9-8. Half-Wave Rectifier Without Centered Ground and Center-Tapped Secondary Performs Voltage Doubling Twice, Hence Quadrupling V_{IN}

9.2.3.2 Recommended Transformers

Table 9-3 shows recommended transformer designs for SN6507, providing high effciency, optimized EMI peformance and small form factor at low-cost.

Table 9-3. Recommended Center Tapped Transformers for SN6507

APPLICATION	TURNS RATIO (1:N)	V-t product Min (Vμs)	ISOLATION (V_{RMS})	DIMENSION (mm) (L,W,H)	PART NUMBER [1]
24 V→ 15 V, 500 mA	0.73	15	2.5 k	(8.5, 12.87, 5.16)	Wurth 750319696
	0.71	30	2.5 k	(10.3, 12.07, 5.97)	Coilcraft ZB1459-BE
	0.73	25	2.5 k	(11.8, 13.2, 11.1)	Bourns SM91207L-E
	0.75	25	3.75 k	(10.3, 13.2, 12.5)	Pulse PAG6356.086NLT
12 V→ 15 V, 500 mA	1.4	22	2.5 k	(10.3, 12.07, 5.97)	Coilcraft ZB1445-CE
	1.4	22	2.5 k	(8.5, 12.87, 5.16)	Wurth 750319692
	1.2	15	2.5 k	(11.8, 13.2, 11.1)	Bourns SM91208L-E
24 V→ 30 V, 500 mA	1.4	30	2.5 k	(10.3, 12.07, 5.97)	Coilcraft ZC1891-AE
	1.4	30	2.5 k	(8.5, 12.87, 5.16)	Wurth 750319948
12 V→ 30 V, 500 mA	2.6	22	2.5 k	(8.5, 12.87, 5.16)	Wurth 750319949
	2.8	22	2.5 k	(10.3, 12.07, 5.97)	Coilcraft ZC1892-AE

1. The transformers listed in the table need be verified with SN6507. The transformer specs are preliminary. Please refer to transformer website for final spec

ADVANCE INFORMATION

10 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 3 V and 36 V nominal. If the input supply is located more than a few inches from the device, a 0.1 µF by-pass capacitor should be connected as close as possible to the device V_{CC} pin and a 10 µF capacitor should be connected close to the transformer center-tap pin.

11 Layout

11.1 Layout Guidelines

- The V_{IN} pin must be buffered to ground with a low-ESR ceramic bypass-capacitor. The recommended capacitor value can range from 1 µF to 10 µF. The capacitor must have a voltage rating of 10 V minimum and a X5R or X7R dielectric.
- The optimum placement is closest to the V_{IN} and GND pins at the board entrance to minimize the loop area formed by the bypass-capacitor connection, the V_{IN} terminal, and the GND pin. See Figure 11-1 for a PCB layout example.
- The connections between the device SW1 and SW2 pins and the transformer primary endings, and the connection of the device V_{CC} pin and the transformer center-tap must be as close as possible for minimum trace inductance.
- The connection of the device V_{CC} pin and the transformer center-tap must be buffered to ground with a low-ESR ceramic bypass-capacitor. The recommended capacitor value can range from 1µF to 10 µF. The capacitor must have a voltage rating of 16 V minimum and a X5R or X7R dielectric.
- The device GND pins must be tied to the PCB ground plane using two vias for minimum inductance.
- The ground connections of the capacitors and the ground plane should use two vias for minimum inductance.
- The rectifier diodes should be Schottky diodes with low forward voltage and low capacitance to maximize efficiency.
- The V_{OUT} pin must be buffered to ISO-Ground with a low-ESR ceramic bypass-capacitor. The recommended capacitor value can range from 1µF to 10 µF.

11.2 Layout Example

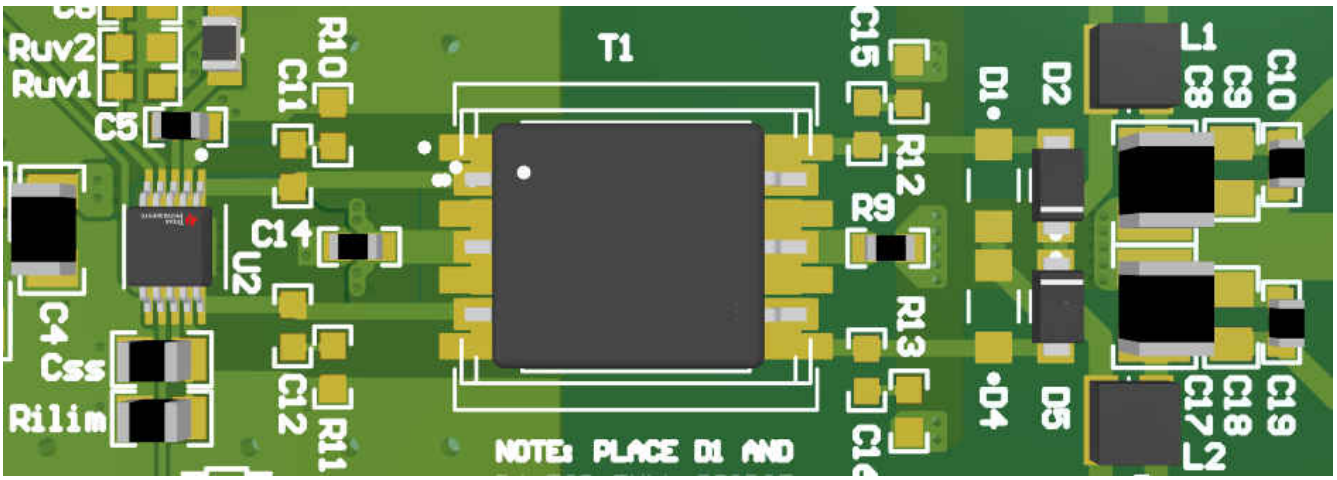


Figure 11-1. Layout Example of a 2-Layer Board

ADVANCE INFORMATION

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Digital Isolator Design Guide*
- Texas Instruments, *Isolation Glossary*
- Texas Instruments, *How to Isolate Signal and Power in Isolated CAN Systems* TI TechNote
- Texas Instruments, *Small Form-Factor Reinforced Isolated IGBT Gate Drive Reference Design for 3-Phase Inverter* TI Design

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

12.4 Trademarks

All trademarks are the property of their respective owners.

13 Mechanical, Packaging, and Orderable Information

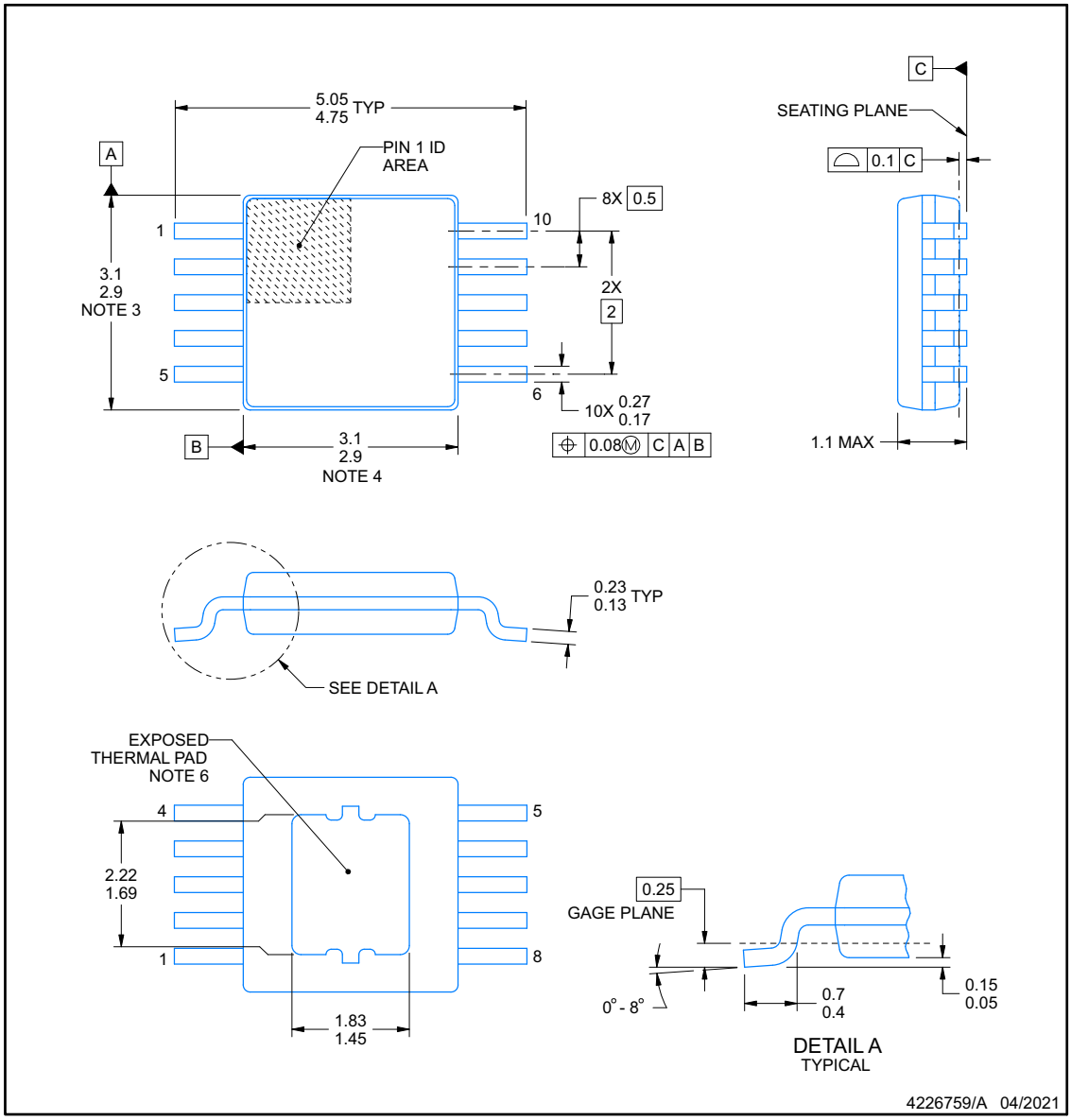
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

DGQ0010D-C01

PowerPAD™ - 1.1 mm max height

PLASTIC SMALL OUTLINE



PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA-T.
6. The thermal pad design could vary depending on manufacturing site.

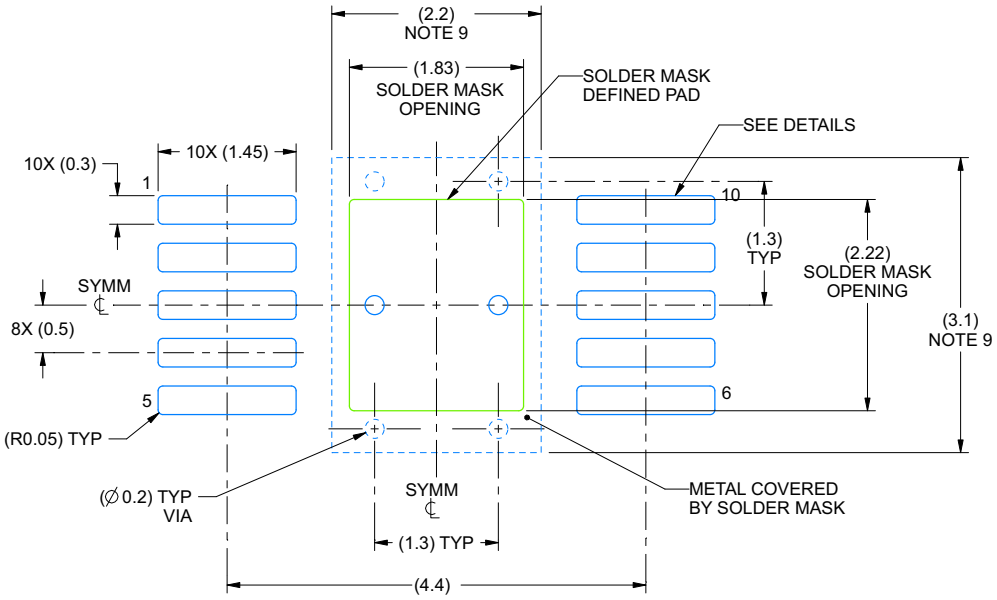
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

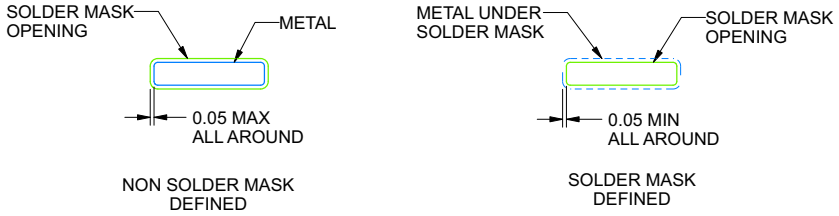
DGQ0010D-C01

PowerPAD ™ - 1.1 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

4226759/A 04/2021

NOTES: (continued)

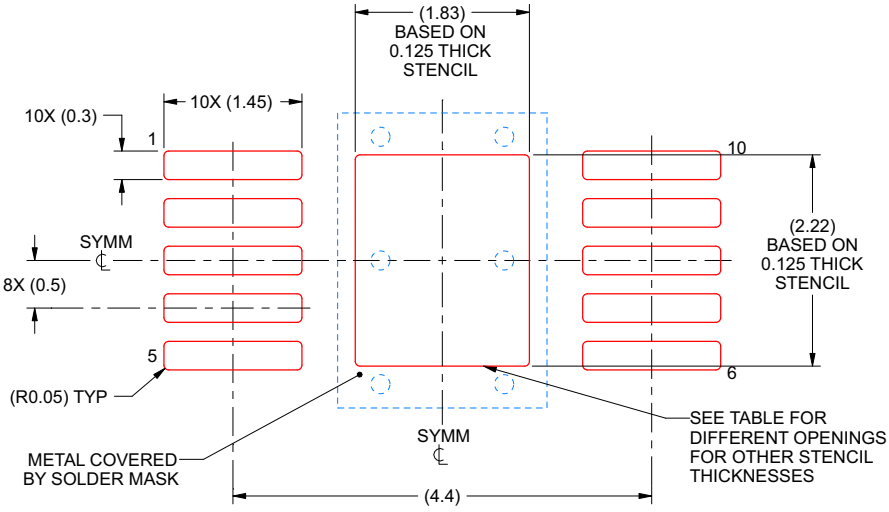
7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
9. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
10. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGQ0010D-C01

PowerPAD ™ - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.05 X 2.48
0.125	1.83 X 2.22 (SHOWN)
0.150	1.67 X 2.03
0.175	1.55 X 1.88

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XSN6507DGQR	ACTIVE	HVSSOP	DGQ	10	2500	TBD	Call TI	Call TI	-55 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

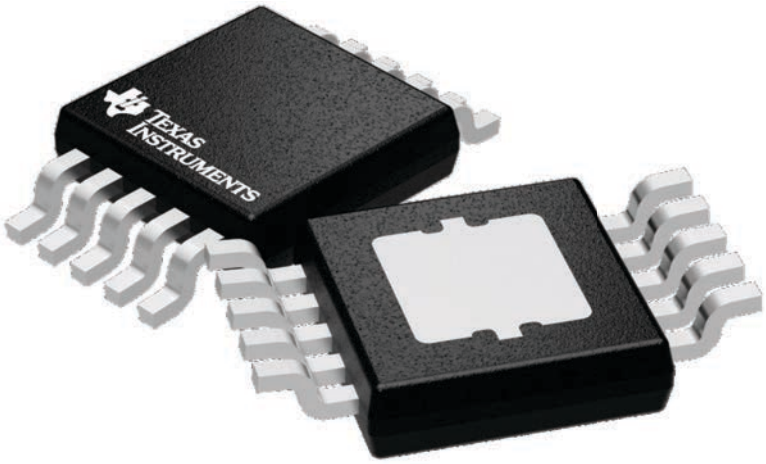
GENERIC PACKAGE VIEW

DGQ 10

PowerPAD™ HVSSOP - 1.1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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