CY7C1471V33

# 72-Mbit (2 M × 36) Flow-Through SRAM with NoBL™ Architecture

## Features

- No Bus Latency™ (NoBL™) architecture eliminates dead cycles between write and read cycles
- Supports up to 133 MHz bus operations with zero wait states
- Data is transferred on every clock
- Pin compatible and functionally equivalent to ZBT™ devices
- Internally self timed output buffer control to eliminate the need to use $\overline{OE}$
- Registered inputs for flow through operation
- Byte Write capability
- 3.3 V/2.5 V I/O supply ($V_{DDQ}$)
- Fast clock-to-output times
  - 6.5 ns (for 133-MHz device)
- Clock enable ($\overline{CEN}$) pin to enable clock and suspend operation
- Synchronous self timed writes
- Asynchronous output enable ($\overline{OE}$)
- CY7C1471V33 available in JEDEC-standard Pb-free 100-pin TQFP
- Three chip enables ($\overline{CE}_1$, $CE_2$, $\overline{CE}_3$) for simple depth expansion
- Automatic power down feature available using ZZ mode or CE deselect
- Burst capability – linear or interleaved burst order
- Low standby power

## Functional Description

The CY7C1471V33 is 3.3 V, 2 M × 36 synchronous flow through burst SRAMs designed specifically to support unlimited true back-to-back read or write operations without the insertion of wait states. The CY7C1471V33 is equipped with the advanced No Bus Latency (NoBL) logic required to enable consecutive read or write operations with data being transferred on every clock cycle. This feature dramatically improves the throughput of data through the SRAM, especially in systems that require frequent write-read transitions.

All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock input is qualified by the clock enable ($\overline{CEN}$) signal, which when deasserted suspends operation and extends the previous clock cycle.Maximum access delay from the clock rise is 6.5 ns (133-MHz device).

Write operations are controlled by two or four byte write select ($BW_X$) and a write enable ($\overline{WE}$) input. All writes are conducted with on-chip synchronous self timed write circuitry.

Three synchronous chip enables ($\overline{CE}_1$, $CE_2$, $\overline{CE}_3$) and an asynchronous output enable ($\overline{OE}$) provide for easy bank selection and output tri-state control. To avoid bus contention, the output drivers are synchronously tri-stated during the data portion of a write sequence.

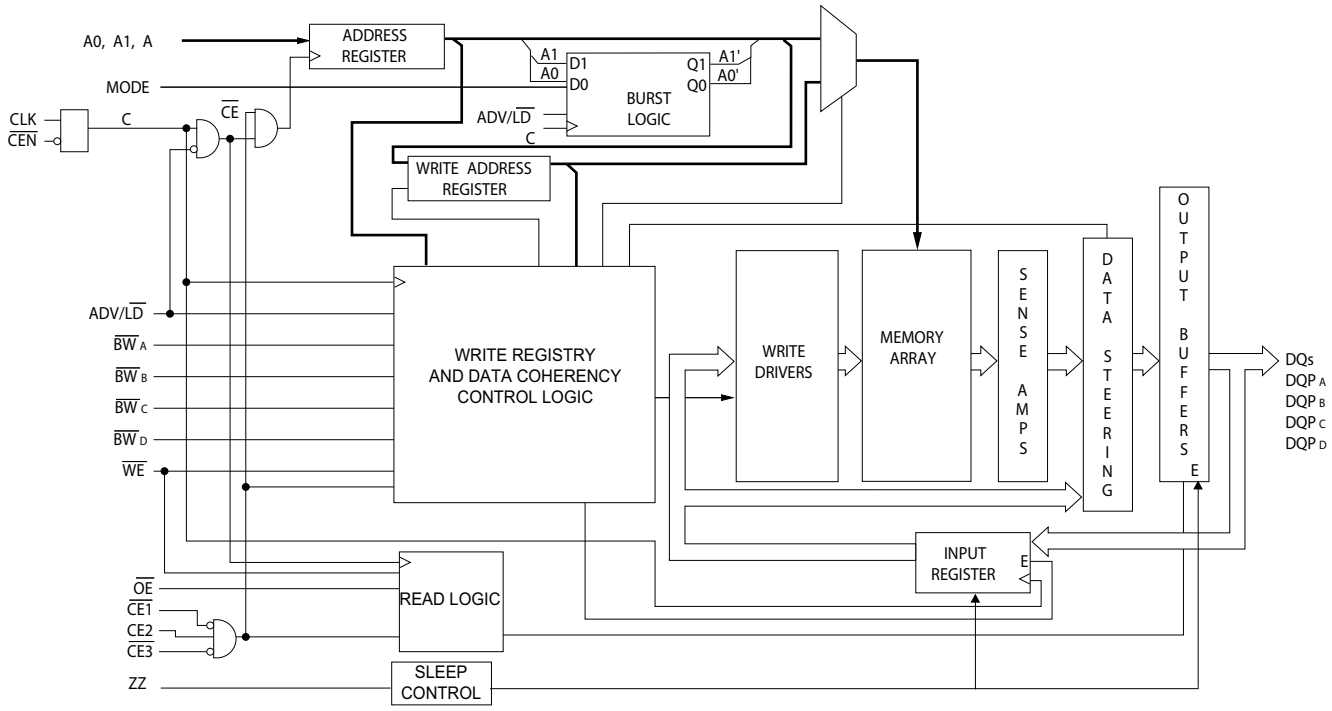
For a complete list of related documentation, click here.

## Selection Guide

| Description | 133 MHz | Unit |
|---|---|---|
| Maximum access time | 6.5 | ns |
| Maximum operating current | 305 | mA |
| Maximum CMOS standby current | 120 | mA |

Errata: For information on silicon errata, see Errata on page 19. Details include trigger conditions, devices affected, and proposed workaround.

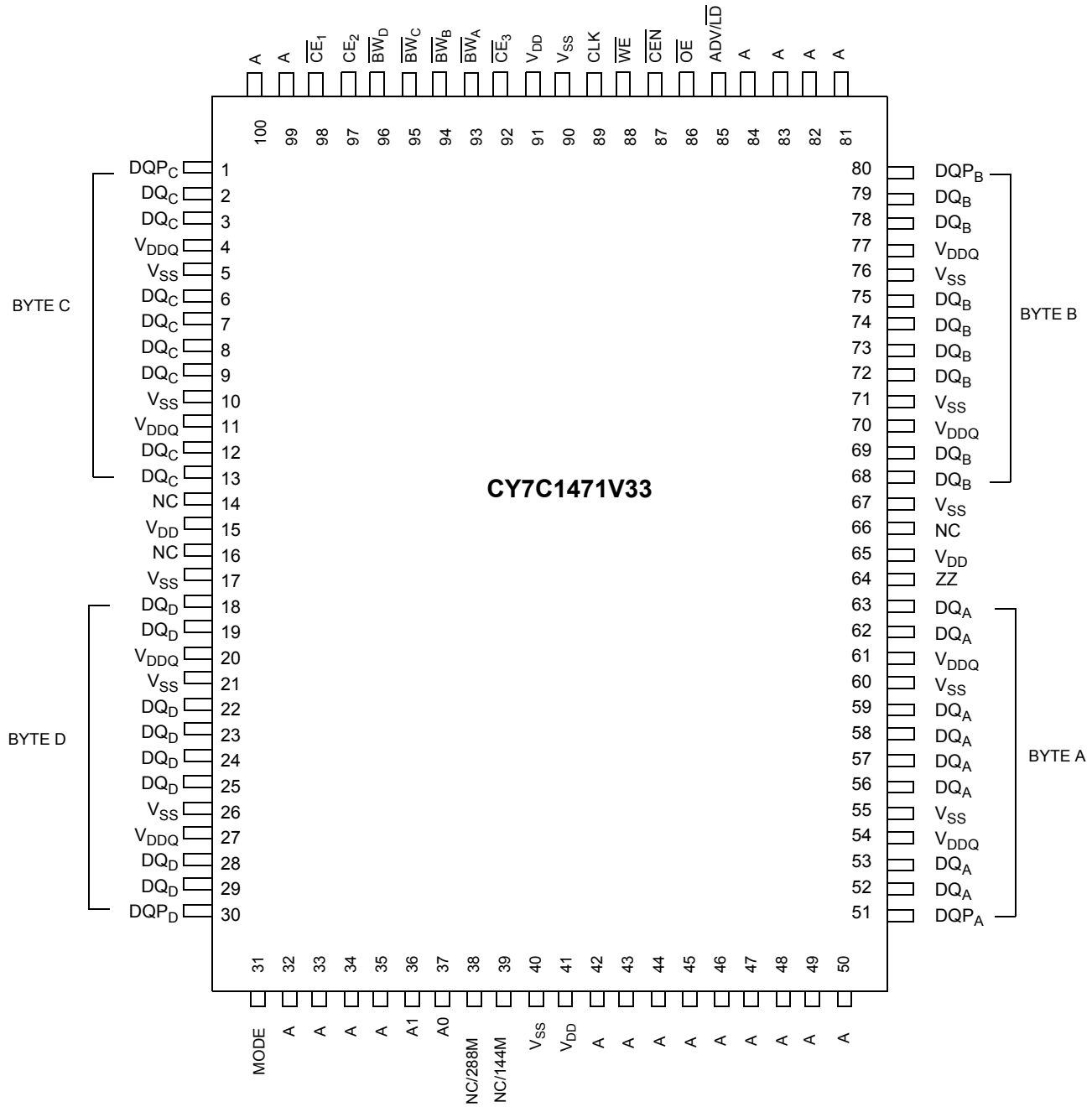
## Logic Block Diagram – CY7C1471V33



## Contents

## Pin Configurations

**Figure 1. 100-pin TQFP (14 × 20 × 1.4 mm) pinout** [1]




**Note**
1. Errata: The ZZ pin (Pin 64) needs to be externally connected to ground. For more information, see Errata on page 19.

## Pin Definitions

| Name | I/O | Description |
|---|---|---|
| $A_0$, $A_1$, A | Input-synchronous | **Address inputs used to select one of the address locations**. Sampled at the rising edge of the CLK. $A_{[1:0]}$ are fed to the two-bit burst counter. |
| $\overline{BW}_A$, $\overline{BW}_B$, $\overline{BW}_C$, $\overline{BW}_D$ | Input-synchronous | **Byte write inputs, active LOW**. Qualified with $\overline{WE}$ to conduct writes to the SRAM. Sampled on the rising edge of CLK. |
| $\overline{WE}$ | Input-synchronous | **Write enable input, active LOW**. Sampled on the rising edge of CLK if $\overline{CEN}$ is active LOW. This signal must be asserted LOW to initiate a write sequence. |
| ADV/$\overline{LD}$ | Input-synchronous | **Advance/load input**. Advances the on-chip address counter or loads a new address. When HIGH (and $\overline{CEN}$ is asserted LOW) the internal burst counter is advanced. When LOW, a new address can be loaded into the device for an access. After being deselected, ADV/$\overline{LD}$ should must driven LOW to load a new address. |
| CLK | Input-clock | **Clock input**. Used to capture all synchronous inputs to the device. CLK is qualified with $\overline{CEN}$. CLK is only recognized if $\overline{CEN}$ is active LOW. |
| $\overline{CE}_1$ | Input-synchronous | **Chip enable 1 input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $CE_2$ and $\overline{CE}_3$ to select or deselect the device. |
| $CE_2$ | Input-synchronous | **Chip enable 2 input, active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$ to select or deselect the device. |
| $\overline{CE}_3$ | Input-synchronous | **Chip enable 3 input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $CE_2$ to select or deselect the device. |
| $\overline{OE}$ | Input-asynchronous | **Output enable, asynchronous input, active LOW**. Combined with the synchronous logic block inside the device to control the direction of the I/O pins. When LOW, the I/O pins are enabled to behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins. $\overline{OE}$ is masked during the data portion of a write sequence, during the first clock when emerging from a deselected state, when the device is deselected. |
| $\overline{CEN}$ | Input-synchronous | **Clock enable input, active LOW**. When asserted LOW the clock signal is recognized by the SRAM. When deasserted HIGH the Clock signal is masked. Since deasserting $\overline{CEN}$ does not deselect the device, use $\overline{CEN}$ to extend the previous cycle when required. |
| ZZ[2] | Input-asynchronous | **ZZ "sleep" input**. This active HIGH input places the device in a non-time critical "sleep" condition with data integrity preserved. During normal operation, this pin must be LOW or left floating. ZZ pin has an internal pull-down. |
| $DQ_s$ | I/O-synchronous | **Bidirectional data I/O lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$. When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, $DQ_s$ and $DQP_X$ are placed in a tri-state condition.The outputs are automatically tri-stated during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of $\overline{OE}$. |
| $DQP_X$ | I/O-synchronous | **Bidirectional data parity I/O lines**. Functionally, these signals are identical to $DQ_s$. During write sequences, $DQP_X$ is controlled by $\overline{BW}_X$ correspondingly. |
| MODE | Input strap pin | **Mode input**. Selects the burst order of the device. When tied to GND selects linear burst sequence. When tied to $V_{DD}$ or left floating selects interleaved burst sequence. |
| $V_{DD}$ | Power supply | **Power supply inputs to the core of the device**. |
| $V_{DDQ}$ | I/O power supply | **Power supply for the I/O circuitry**. |
| $V_{SS}$ | Ground | **Ground for the device**. |
| NC | – | **No connects**. Not internally connected to the die. 144M, 288M, 576M, and 1G are address expansion pins and are not internally connected to the die. |

**Note**
2. Errata: The ZZ pin (Pin 64) needs to be externally connected to ground. For more information, see Errata on page 19.

## Functional Overview

The CY7C1471V33 is synchronous flow through burst SRAMs designed specifically to eliminate wait states during write-read transitions. All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock signal is qualified with the clock enable input signal (CEN). If CEN is HIGH, the clock signal is not recognized and all internal states are maintained. All synchronous operations are qualified with CEN. Maximum access delay from the clock rise ($t_{CDV}$) is 6.5 ns (133-MHz device).

Accesses can be initiated by asserting all three chip enables ($CE_1$, $CE_2$, $\overline{CE_3}$) active at the rising edge of the clock. If (CEN) is active LOW and ADV/LD is asserted LOW, the address presented to the device is latched. The access can either be a read or write operation, depending on the status of the write enable ($\overline{WE}$). Byte write select ($\overline{BW_X}$) can be used to conduct byte write operations.

Write operations are qualified by the write enable ($\overline{WE}$). All writes are simplified with on-chip synchronous self timed write circuitry.

Three synchronous chip enables ($\overline{CE_1}$, $CE_2$, $\overline{CE_3}$) and an asynchronous output enable ($\overline{OE}$) simplify depth expansion. All operations (reads, writes, and deselects) are pipelined. ADV/$\overline{LD}$ must be driven LOW after the device is deselected to load a new address for the next operation.

### Single Read Accesses

A read access is initiated when these conditions are satisfied at clock rise:

- $\overline{CEN}$ is asserted LOW
- $\overline{CE_1}$, $CE_2$, and $\overline{CE_3}$ are all asserted active
- $\overline{WE}$ is deasserted HIGH
- ADV/$\overline{LD}$ is asserted LOW.

The address presented to the address inputs is latched into the address register and presented to the memory array and control logic. The control logic determines that a read access is in progress and allows the requested data to propagate to the output buffers. The data is available within 6.5 ns (133-MHz device) provided $\overline{OE}$ is active LOW. After the first clock of the read access, the output buffers are controlled by $\overline{OE}$ and the internal control logic. $\overline{OE}$ must be driven LOW to drive out the requested data. On the subsequent clock, another operation (read/write/deselect) can be initiated. When the SRAM is deselected at clock rise by one of the chip enable signals, output is be tri-stated immediately.

### Burst Read Accesses

The CY7C1471V33 have an on-chip burst counter that enables the user to supply a single address and conduct up to four reads without reasserting the address inputs. ADV/$\overline{LD}$ must be driven LOW to load a new address into the SRAM, as described in the Single Read Accesses section. The sequence of the burst counter is determined by the MODE input signal. A LOW input on MODE selects a linear burst mode, a HIGH selects an interleaved burst sequence. Both burst counters use A0 and A1 in the burst sequence, and wraps around when incremented sufficiently. A HIGH input on ADV/$\overline{LD}$ increments the internal burst counter regardless of the state of chip enable inputs or $\overline{WE}$. $\overline{WE}$ is latched at the beginning of a burst cycle. Therefore, the type of access (read or write) is maintained throughout the burst sequence.

### Single Write Accesses

Write accesses are initiated when the following conditions are satisfied at clock rise: (1) $\overline{CEN}$ is asserted LOW, (2) $\overline{CE_1}$, $CE_2$, and $\overline{CE_3}$ are all asserted active, and (3) $\overline{WE}$ is asserted LOW. The address presented to the address bus is loaded into the Address Register. The Write signals are latched into the Control Logic block. The data lines are automatically tri-stated regardless of the state of the $\overline{OE}$ input signal. This allows the external logic to present the data on DQs and $DQP_X$.

On the next clock rise the data presented to DQs and $DQP_X$ (or a subset for Byte Write operations, see Truth Table for Read/Write on page 9 for details) inputs is latched into the device and the write is complete. Additional accesses (read/write/deselect) can be initiated on this cycle.

The data written during the write operation is controlled by $\overline{BW_X}$ signals. The CY7C1471V33 provides Byte Write capability that is described in the Truth Table for Read/Write on page 9. The input $\overline{WE}$ with the selected $\overline{BW_X}$ input selectively writes to only the desired bytes. Bytes not selected during a byte write operation remain unaltered. A synchronous self timed write mechanism has been provided to simplify the write operations. Byte write capability is included to greatly simplify read/modify/write sequences, which can be reduced to simple byte write operations.

Because the CY7C1471V33 are common I/O devices, data must not be driven into the device while the outputs are active. The output enable ($\overline{OE}$) can be deasserted HIGH before presenting data to the DQs and $DQP_X$ inputs. Doing so tri-states the output drivers. As a safety precaution, DQs and $DQP_X$ are automatically tri-stated during the data portion of a write cycle, regardless of the state of $\overline{OE}$.

### Burst Write Accesses

The CY7C1471V33 have an on-chip burst counter that enables the user to supply a single address and conduct up to four write operations without reasserting the address inputs. ADV/$\overline{LD}$ must be driven LOW to load the initial address, as described in the Single Write Accesses section. When ADV/$\overline{LD}$ is driven HIGH on the subsequent clock rise, the chip enables ($\overline{CE_1}$, $CE_2$, and $\overline{CE_3}$) and $\overline{WE}$ inputs are ignored and the burst counter is incremented. The correct $\overline{BW_X}$ inputs must be driven in each cycle of the burst write to write the correct bytes of data.

### Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation “sleep” mode. Two clock cycles are required to enter into or exit from this “sleep” mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the “sleep” mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected before entering the “sleep” mode. $\overline{CE_1}$, $CE_2$, and $\overline{CE_3}$, must remain inactive for the duration of $t_{ZZREC}$ after the ZZ input returns LOW.

### Interleaved Burst Address Table

(MODE = Floating or $V_{DD}$)

| First Address A1:A0 | Second Address A1:A0 | Third Address A1:A0 | Fourth Address A1:A0 |
|---|---|---|---|
| 00 | 01 | 10 | 11 |
| 01 | 00 | 11 | 10 |
| 10 | 11 | 00 | 01 |
| 11 | 10 | 01 | 00 |

### Linear Burst Address Table

(MODE = GND)

| First Address A1:A0 | Second Address A1:A0 | Third Address A1:A0 | Fourth Address A1:A0 |
|---|---|---|---|
| 00 | 01 | 10 | 11 |
| 01 | 10 | 11 | 00 |
| 10 | 11 | 00 | 01 |
| 11 | 00 | 01 | 10 |

### ZZ Mode Electrical Characteristics

| Parameter | Description | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $I_{DDZZ}$ | Sleep mode standby current | ZZ $\geq V_{DD} - 0.2$ V | – | 120 | mA |
| $t_{ZZS}$ | Device operation to ZZ | ZZ $\geq V_{DD} - 0.2$ V | – | $2t_{CYC}$ | ns |
| $t_{ZZREC}$ | ZZ recovery time | ZZ $\leq$ 0.2 V | $2t_{CYC}$ | – | ns |
| $t_{ZZI}$ | ZZ active to sleep current | This parameter is sampled | – | $2t_{CYC}$ | ns |
| $t_{RZZI}$ | ZZ Inactive to exit sleep current | This parameter is sampled | 0 | – | ns |

## Truth Table

The truth table for CY7C1471V33 follows. [3, 4, 5, 6, 7, 8, 9]

| Operation | Address Used | $\overline{CE}_1$ | $CE_2$ | $\overline{CE}_3$ | ZZ | ADV/$\overline{LD}$ | $\overline{WE}$ | $\overline{BW}_X$ | $\overline{OE}$ | $\overline{CEN}$ | CLK | DQ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Deselect cycle | None | H | X | X | L | L | X | X | X | L | L->H | Tri-state |
| Deselect cycle | None | X | X | H | L | L | X | X | X | L | L->H | Tri-state |
| Deselect cycle | None | X | L | X | L | L | X | X | X | L | L->H | Tri-state |
| Continue deselect cycle | None | X | X | X | L | H | X | X | X | L | L->H | Tri-state |
| Read cycle (begin burst) | External | L | H | L | L | L | H | X | L | L | L->H | Data out (Q) |
| Read cycle (continue burst) | Next | X | X | X | L | H | X | X | L | L | L->H | Data out (Q) |
| NOP/dummy read (begin burst) | External | L | H | L | L | L | H | X | H | L | L->H | Tri-state |
| Dummy read (continue burst) | Next | X | X | X | L | H | X | X | H | L | L->H | Tri-state |
| Write cycle (begin burst) | External | L | H | L | L | L | L | L | X | L | L->H | Data in (D) |
| Write cycle (continue burst) | Next | X | X | X | L | H | X | L | X | L | L->H | Data in (D) |
| NOP/write abort (begin burst) | None | L | H | L | L | L | L | H | X | L | L->H | Tri-state |
| Write abort (continue burst) | Next | X | X | X | L | H | X | H | X | L | L->H | Tri-state |
| Ignore clock edge (stall) | Current | X | X | X | L | X | X | X | X | H | L->H | – |
| Sleep mode | None | X | X | X | H | X | X | X | X | X | X | Tri-state |

**Notes**
3. X = “Don't Care.” H = Logic HIGH, L = Logic LOW. $\overline{BW}_X$ = L signifies at least one byte write select is active, $\overline{BW}_X$ = valid signifies that the desired byte write selects are asserted, see Truth Table for Read/Write on page 9 for details.
4. Write is defined by $\overline{BW}_X$, and $\overline{WE}$. See Truth Table for Read/Write on page 9.
5. When a Write cycle is detected, all I/Os are tri-stated, even during byte writes.
6. The DQs and $DQP_X$ pins are controlled by the current cycle and the $\overline{OE}$ signal. $\overline{OE}$ is asynchronous and is not sampled with the clock.
7. $\overline{CEN}$ = H, inserts wait states.
8. Device powers up deselected with the I/Os in a tri-state condition, regardless of $\overline{OE}$.
9. $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle DQs and $DQP_X$ = tri-state when $\overline{OE}$ is inactive or when the device is deselected, and DQs and $DQP_X$ = data when $\overline{OE}$ is active.

## Truth Table for Read/Write

The read-write truth table for CY7C1471V33 follows. [10, 11, 12]

| Function | $\overline{WE}$ | $\overline{BW_A}$ | $\overline{BW_B}$ | $\overline{BW_C}$ | $\overline{BW_D}$ |
|---|---|---|---|---|---|
| Read | H | X | X | X | X |
| Write no bytes written | L | H | H | H | H |
| Write byte A – ($DQ_A$ and $DQP_A$) | L | L | H | H | H |
| Write byte B – ($DQ_B$ and $DQP_B$) | L | H | L | H | H |
| Write byte C – ($DQ_C$ and $DQP_C$) | L | H | H | L | H |
| Write byte D – ($DQ_D$ and $DQP_D$) | L | H | H | H | L |
| Write all bytes | L | L | L | L | L |

**Notes**
10. X = “Don't Care.” H = Logic HIGH, L = Logic LOW. $\overline{BW_X}$ = L signifies at least one byte write select is active, $\overline{BW_X}$ = valid signifies that the desired byte write selects are asserted, see Truth Table for Read/Write for details.
11. Write is defined by $\overline{BW_X}$, and $\overline{WE}$. See Truth Table for Read/Write.
12. Table only lists a partial listing of the byte write combinations. Any combination of $\overline{BW_X}$ is valid. Appropriate write is based on which byte write is active.

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage on $V_{DD}$ relative to GND .....–0.5 V to +4.6 V

Supply voltage on $V_{DDQ}$ relative to GND ..... –0.5 V to +$V_{DD}$

DC voltage applied to outputs in tri-state .....–0.5 V to $V_{DDQ}$ + 0.5 V

DC input voltage .....–0.5 V to $V_{DD}$ + 0.5 V

Current into outputs (LOW) ..... 20 mA

Static discharge voltage (MIL-STD-883, method 3015) ..... > 2001 V

Latch-up current ..... > 200 mA

## Operating Range

| Range | Ambient Temperature | $V_{DD}$ | $V_{DDQ}$ |
|---|---|---|---|
| Commercial | 0 °C to +70 °C | 3.3 V – 5% / + 10% | 2.5 V – 5% to $V_{DD}$ |

## Electrical Characteristics

Over the Operating Range

| Parameter [13, 14] | Description | Test Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Power supply voltage | | | 3.135 | 3.6 | V |
| $V_{DDQ}$ | I/O supply voltage | For 3.3 V I/O | | 3.135 | $V_{DD}$ | V |
| | | For 2.5 V I/O | | 2.375 | 2.625 | V |
| $V_{OH}$ | Output HIGH voltage | For 3.3 V I/O, $I_{OH}$ = –4.0 mA | | 2.4 | – | V |
| | | For 2.5 V I/O, $I_{OH}$ = –1.0 mA | | 2.0 | – | V |
| $V_{OL}$ | Output LOW voltage | For 3.3 V I/O, $I_{OL}$ = 8.0 mA | | – | 0.4 | V |
| | | For 2.5 V I/O, $I_{OL}$ = 1.0 mA | | – | 0.4 | V |
| $V_{IH}$ | Input HIGH voltage [13] | For 3.3 V I/O | | 2.0 | $V_{DD}$ + 0.3 V | V |
| | | For 2.5 V I/O | | 1.7 | $V_{DD}$ + 0.3 V | V |
| $V_{IL}$ | Input LOW voltage [13] | For 3.3 V I/O | | –0.3 | 0.8 | V |
| | | For 2.5 V I/O | | –0.3 | 0.7 | V |
| $I_X$ | Input leakage current except ZZ and MODE | GND ≤ $V_I$ ≤ $V_{DDQ}$ | | –5 | 5 | µA |
| | Input current of MODE | Input = $V_{SS}$ | | –30 | – | µA |
| | | Input = $V_{DD}$ | | – | 5 | µA |
| | Input current of ZZ | Input = $V_{SS}$ | | –5 | – | µA |
| | | Input = $V_{DD}$ | | – | 30 | µA |
| $I_{OZ}$ | Output leakage current | GND ≤ $V_I$ ≤ $V_{DD}$, output disabled | | –5 | 5 | µA |
| $I_{DD}$ | $V_{DD}$ operating supply current | $V_{DD}$ = Max, $I_{OUT}$ = 0 mA, f = $f_{MAX}$ = 1/$t_{CYC}$ | 7.5 ns cycle, 133 MHz | – | 305 | mA |
| $I_{SB1}$ | Automatic CE power-down current – TTL inputs | $V_{DD}$ = Max, device deselected, $V_{IN}$ ≥ $V_{IH}$ or $V_{IN}$ ≤ $V_{IL}$, f = $f_{MAX}$, inputs switching | 7.5 ns cycle, 133 MHz | – | 200 | mA |
| $I_{SB2}$ | Automatic CE power-down current – CMOS inputs | $V_{DD}$ = Max, device deselected, $V_{IN}$ ≤ 0.3 V or $V_{IN}$ ≥ $V_{DD}$ – 0.3 V, f = 0, inputs static | 7.5 ns cycle, 133 MHz | – | 120 | mA |
| $I_{SB3}$ | Automatic CE power-down current – CMOS inputs | $V_{DD}$ = Max, device deselected, $V_{IN}$ ≤ 0.3 V or $V_{IN}$ ≥ $V_{DDQ}$ – 0.3 V, f = $f_{MAX}$, inputs switching | 7.5 ns cycle, 133 MHz | – | 200 | mA |
| $I_{SB4}$ | Automatic CE power-down current – TTL inputs | $V_{DD}$ = Max, device deselected, $V_{IN}$ ≥ $V_{DD}$ – 0.3 V or $V_{IN}$ ≤ 0.3 V, f = 0, inputs static | 7.5 ns cycle, 133 MHz | – | 165 | mA |

**Notes**

13. Overshoot: $V_{IH(AC)}$ < $V_{DD}$ + 1.5 V (pulse width less than $t_{CYC}$/2). Undershoot: $V_{IL(AC)}$ > –2 V (pulse width less than $t_{CYC}$/2).
14. $T_{Power\text{-}up}$: assumes a linear ramp from 0 V to $V_{DD(min)}$ within 200 ms. During this time $V_{IH}$ < $V_{DD}$ and $V_{DDQ}$ ≤ $V_{DD}$.

## Capacitance

| Parameter [15] | Description | Test Conditions | 100-pin TQFP Package | Unit |
|---|---|---|---|---|
| $C_{ADDRESS}$ | Address input capacitance | $T_A$ = 25 °C, f = 1 MHz, $V_{DD}$ = 3.3 V, $V_{DDQ}$ = 2.5 V | 6 | pF |
| $C_{DATA}$ | Data input capacitance | | 5 | pF |
| $C_{CTRL}$ | Control input capacitance | | 8 | pF |
| $C_{CLK}$ | Clock input capacitance | | 6 | pF |
| $C_{IO}$ | Input/Output capacitance | | 5 | pF |

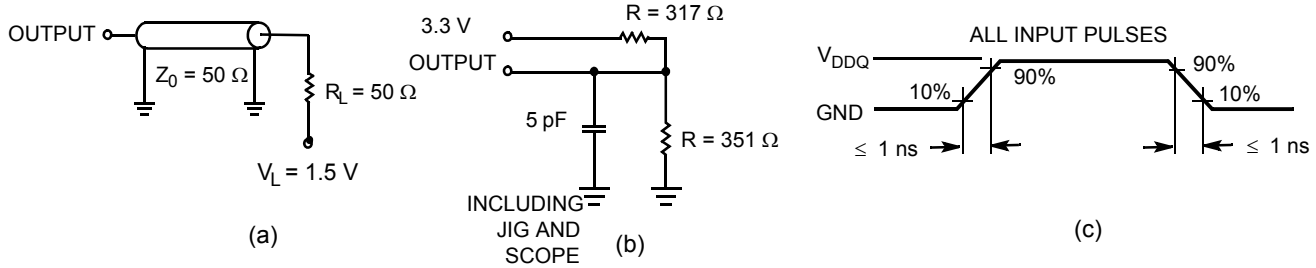
## Thermal Resistance

| Parameter [15] | Description | Test Conditions | 100-pin TQFP Max | Unit |
|---|---|---|---|---|
| $\Theta_{JA}$ | Thermal resistance (junction to ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance, according to EIA/JESD51. | 24.63 | °C/W |
| $\Theta_{JC}$ | Thermal resistance (junction to case) | | 2.28 | °C/W |

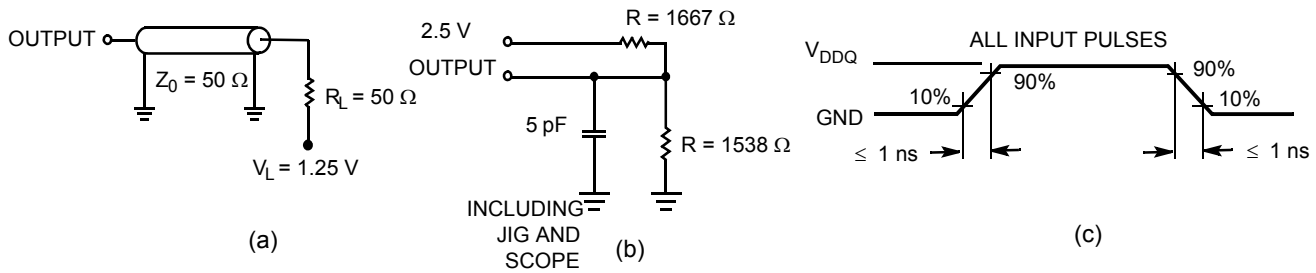
## AC Test Loads and Waveforms

**Figure 2. AC Test Loads and Waveforms**

**3.3 V I/O Test Load**




**2.5 V I/O Test Load**




**Note**
15. Tested initially and after any design or process change that may affect these parameters.

## Switching Characteristics

Over the Operating Range

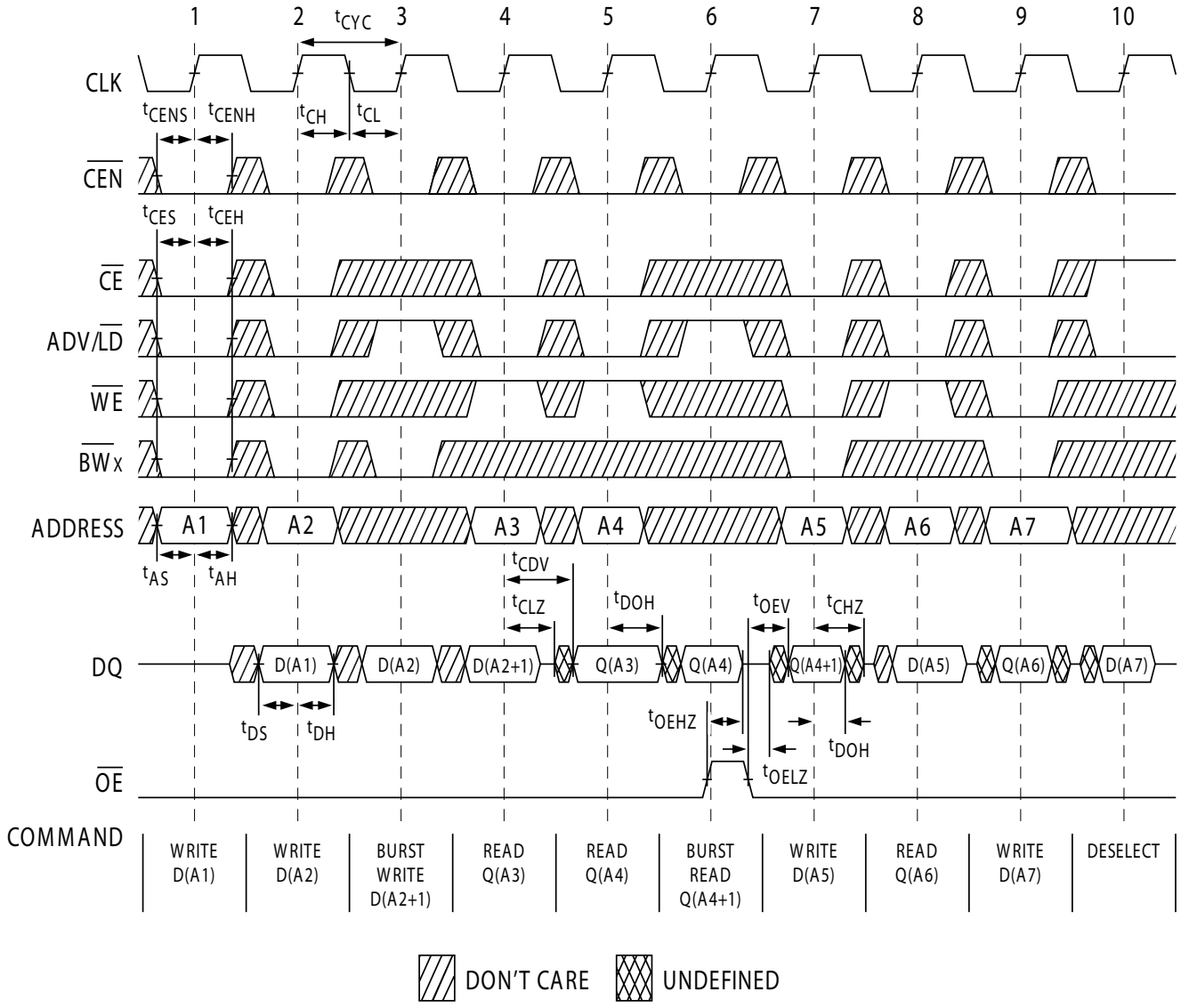
| Parameter [16, 17] | Description | 133 MHz | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| $t_{POWER}$ [18] | | 1 | – | ms |
| **Clock** | | | | |
| $t_{CYC}$ | Clock cycle time | 7.5 | – | ns |
| $t_{CH}$ | Clock HIGH | 2.5 | – | ns |
| $t_{CL}$ | Clock LOW | 2.5 | – | ns |
| **Output Times** | | | | |
| $t_{CDV}$ | Data output valid after CLK rise | – | 6.5 | ns |
| $t_{DOH}$ | Data output hold after CLK rise | 2.5 | – | ns |
| $t_{CLZ}$ | Clock to low Z [19, 20, 21] | 3.0 | – | ns |
| $t_{CHZ}$ | Clock to high Z [19, 20, 21] | – | 3.8 | ns |
| $t_{OEV}$ | $\overline{OE}$ LOW to output valid | – | 3.0 | ns |
| $t_{OELZ}$ | $\overline{OE}$ LOW to output low Z [19, 20, 21] | 0 | – | ns |
| $t_{OEHZ}$ | $\overline{OE}$ HIGH to output high Z [19, 20, 21] | – | 3.0 | ns |
| **Setup Times** | | | | |
| $t_{AS}$ | Address setup before CLK rise | 1.5 | – | ns |
| $t_{ALS}$ | ADV/$\overline{LD}$ setup before CLK rise | 1.5 | – | ns |
| $t_{WES}$ | $\overline{WE}$, $\overline{BW}_X$ setup before CLK rise | 1.5 | – | ns |
| $t_{CENS}$ | $\overline{CEN}$ setup before CLK rise | 1.5 | – | ns |
| $t_{DS}$ | Data input setup before CLK rise | 1.5 | – | ns |
| $t_{CES}$ | Chip enable setup before CLK rise | 1.5 | – | ns |
| **Hold Times** | | | | |
| $t_{AH}$ | Address hold after CLK rise | 0.5 | – | ns |
| $t_{ALH}$ | ADV/$\overline{LD}$ hold after CLK rise | 0.5 | – | ns |
| $t_{WEH}$ | $\overline{WE}$, $\overline{BW}_X$ hold after CLK rise | 0.5 | – | ns |
| $t_{CENH}$ | $\overline{CEN}$ hold after CLK rise | 0.5 | – | ns |
| $t_{DH}$ | Data input hold after CLK rise | 0.5 | – | ns |
| $t_{CEH}$ | Chip enable hold after CLK rise | 0.5 | – | ns |

**Notes**

16. Unless otherwise noted in the following table, timing reference level is 1.5 V when $V_{DDQ}$ = 3.3 V and is 1.25 V when $V_{DDQ}$ = 2.5 V.
17. Test conditions shown in (a) of Figure 2 on page 11 unless otherwise noted.
18. This part has an internal voltage regulator; $t_{POWER}$ is the time that the power needs to be supplied above $V_{DD(minimum)}$ initially, before a read or write operation can be initiated.
19. $t_{CHZ}$, $t_{CLZ}$, $t_{OELZ}$, and $t_{OEHZ}$ are specified with AC test conditions shown in part (b) ofFigure 2 on page 11. Transition is measured ±200 mV from steady-state voltage.
20. At any supplied voltage and temperature, $t_{OEHZ}$ is less than $t_{OELZ}$ and $t_{CHZ}$ is less than $t_{CLZ}$ to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve high Z before low Z under the same system conditions.
21. This parameter is sampled and not 100% tested.

## Switching Waveforms

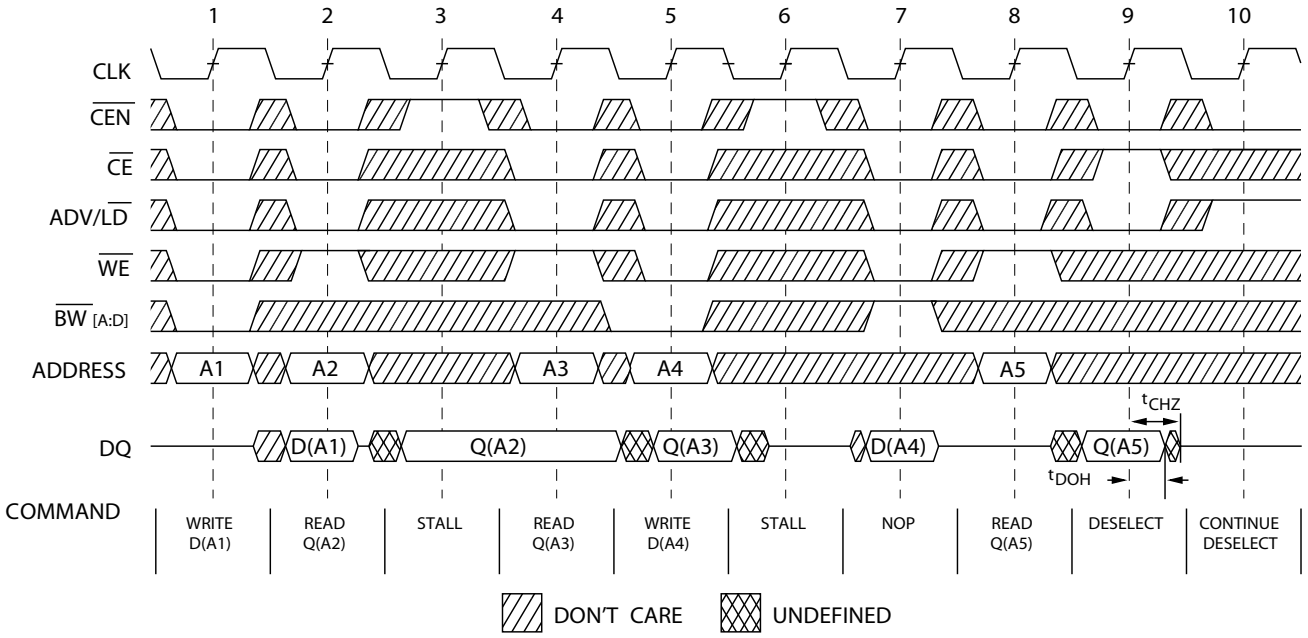
**Figure 3. Read/Write Timing** [22, 23, 24]




**Notes**
22. For this waveform ZZ is tied LOW.
23. When $\overline{CE}$ is LOW, $\overline{CE}_1$ is LOW, $CE_2$ is HIGH, and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH, $\overline{CE}_1$ is HIGH, $CE_2$ is LOW or $\overline{CE}_3$ is HIGH.
24. Order of the burst sequence is determined by the status of the MODE (0 = Linear, 1 = Interleaved). Burst operations are optional.

## Switching Waveforms *(continued)*

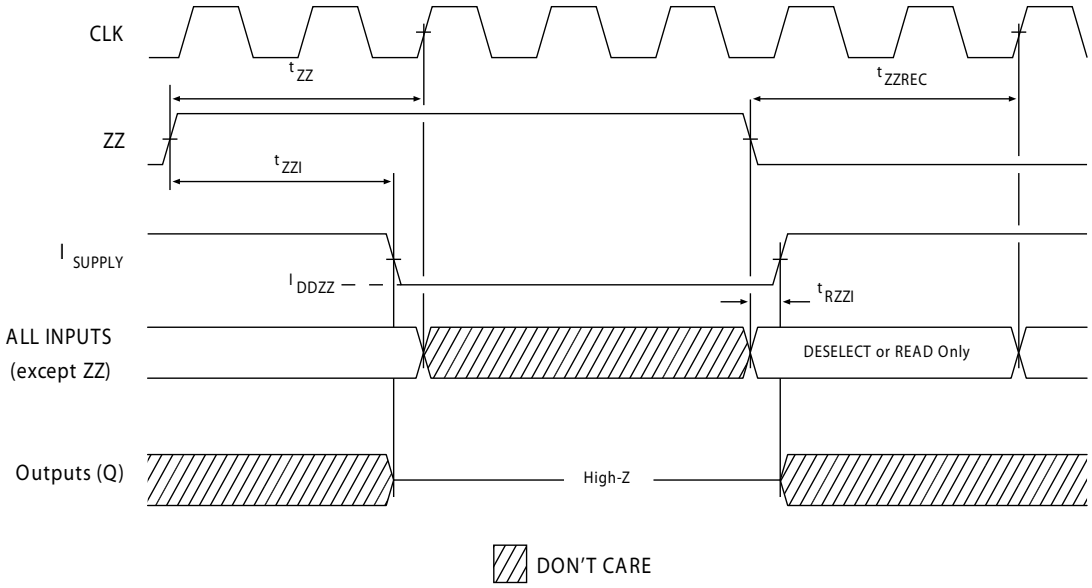
**Figure 4. NOP, STALL and DESELECT Cycles** [25, 26, 27]




**Notes**
25. For this waveform ZZ is tied LOW.
26. When $\overline{CE}$ is LOW, $\overline{CE_1}$ is LOW, $CE_2$ is HIGH, and $\overline{CE_3}$ is LOW. When $\overline{CE}$ is HIGH, $\overline{CE_1}$ is HIGH, $CE_2$ is LOW or $\overline{CE_3}$ is HIGH.
27. The IGNORE CLOCK EDGE or STALL cycle (Clock 3) illustrates $\overline{CEN}$ being used to create a pause. A write is not performed during this cycle.

## Switching Waveforms *(continued)*

**Figure 5. ZZ Mode Timing** [28, 29]



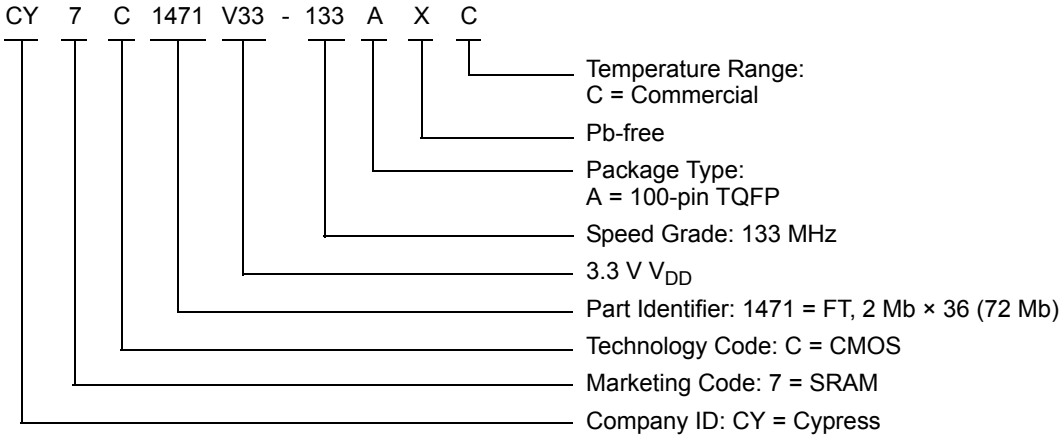

**Notes**
28. Device must be deselected when entering ZZ mode. See Truth Table on page 8 for all possible signal conditions to deselect the device.
29. DQs are in high Z when exiting ZZ sleep mode.

## Ordering Information

Cypress offers other versions of this type of product in many different configurations and features. The below table contains only the list of parts that are currently available. For a complete listing of all options, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products or contact your local sales representative. Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives and distributors. To find the office closest to you, visit us at http://www.cypress.com/go/datasheet/offices.

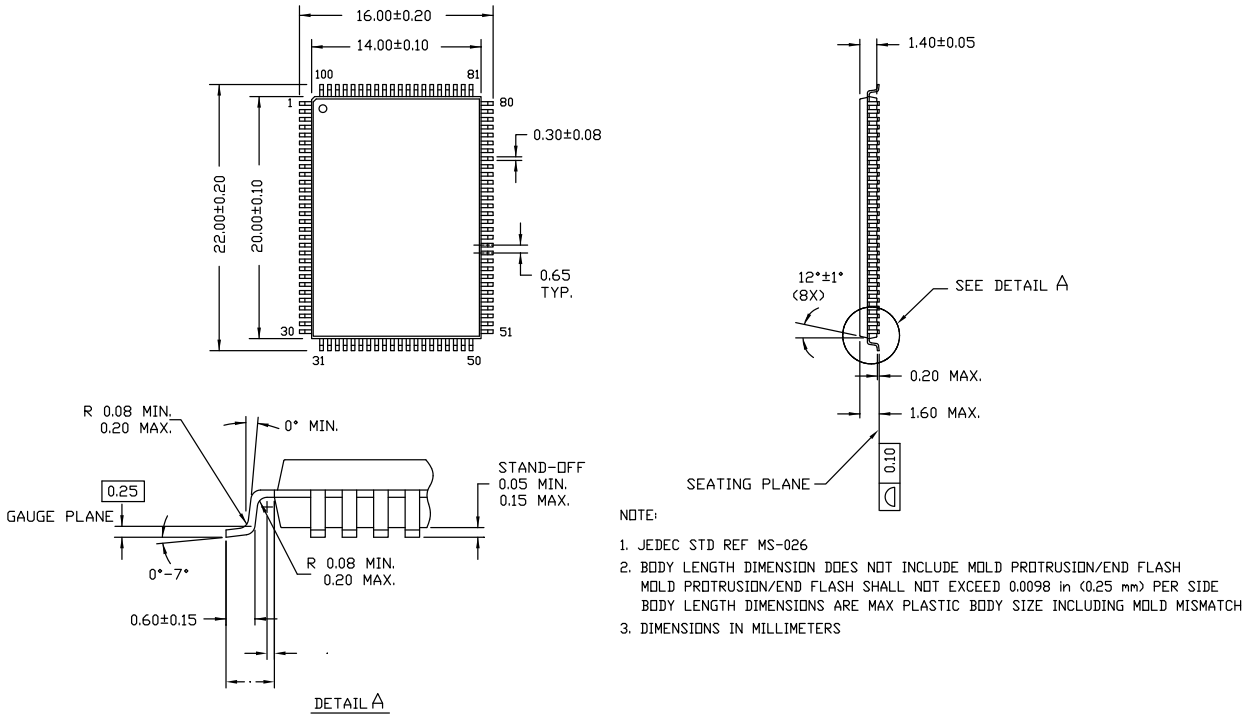
| Speed (MHz) | Ordering Code | Package Diagram | Part and Package Type | Operating Range |
|---|---|---|---|---|
| 133 | CY7C1471V33-133AXC | 51-85050 | 100-pin TQFP (14 × 20 × 1.4 mm) Pb-free | Commercial |

### Ordering Code Definitions



## Package Diagrams

**Figure 6. 100-pin TQFP (14 × 20 × 1.4 mm) A100RA Package Outline, 51-85050**




NOTE:

1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
   MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE
   BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS

51-85050 *E

## Acronyms

| Acronym | Description |
|---|---|
| CMOS | Complementary Metal Oxide Semiconductor |
| $\overline{CE}$ | Chip Enable |
| $\overline{CEN}$ | Clock Enable |
| I/O | Input/Output |
| JEDEC | Joint Electron Devices Engineering Council |
| NoBL | No Bus Latency |
| $\overline{OE}$ | Output Enable |
| SRAM | Static Random Access Memory |
| TQFP | Thin Quad Flat Pack |
| TTL | Transistor-Transistor Logic |
| $\overline{WE}$ | Write Enable |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|---|---|
| °C | degree Celsius |
| MHz | megahertz |
| µA | microampere |
| mA | milliampere |
| mm | millimeter |
| ms | millisecond |
| mV | millivolt |
| ns | nanosecond |
| Ω | ohm |
| % | percent |
| pF | picofarad |
| V | volt |
| W | watt |

# Errata

This section describes the Ram9 NoBL ZZ pin issue. Details include trigger conditions, the devices affected, proposed workaround and silicon revision applicability. Please contact your local Cypress sales representative if you have further questions.

## Part Numbers Affected

| Density & Revision | Package Type | Operating Range |
|---|---|---|
| 72Mb-Ram9 NoBL SRAMs: CY7C147*V33 | 100-pin TQFP | Commercial |

## Product Status

All of the devices in the Ram9 72Mb NoBL family are qualified and available in production quantities.

## Ram9 NoBL ZZ Pin Issues Errata Summary

The following table defines the errata applicable to available Ram9 72Mb NoBL family devices.

| Item | Issues | Description | Device | Fix Status |
|---|---|---|---|---|
| 1. | ZZ Pin | When asserted HIGH, the ZZ pin places device in a “sleep” condition with data integrity preserved.The ZZ pin currently does not have an internal pull-down resistor and hence cannot be left floating externally by the user during normal mode of operation. | 72M-Ram9 (90nm) | For the 72M Ram9 (90 nm) devices, this issue was fixed in the new revision. Please contact your local sales rep for availability. |

### 1. ZZ Pin Issue

- PROBLEM DEFINITION
  The problem occurs only when the device is operated in the normal mode with ZZ pin left floating. The ZZ pin on the SRAM device does not have an internal pull-down resistor. Switching noise in the system may cause the SRAM to recognize a HIGH on the ZZ input, which may cause the SRAM to enter sleep mode. This could result in incorrect or undesirable operation of the SRAM.

- TRIGGER CONDITIONS
  Device operated with ZZ pin left floating.

- SCOPE OF IMPACT
  When the ZZ pin is left floating, the device delivers incorrect data.

- WORKAROUND
  Tie the ZZ pin externally to ground.

- FIX STATUS
  Fix was done for the 72M RAM9 NoBL SRAMs devices. Fixed devices have a new revision. The following table lists the devices affected and the new revision after the fix.

**Table 1. List of Affected Devices and the new revision**

| Revision before the Fix | New Revision after the Fix |
|---|---|
| CY7C147*V33 | CY7C147*BV33 |

## Document History Page

| Document Title: CY7C1471V33, 72-Mbit (2 M × 36) Flow-Through SRAM with NoBL™ Architecture<br>Document Number: 38-05288 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| ** | 114675 | PKS | 08/06/02 | New data sheet. |
| *A | 121521 | CJM | 02/07/03 | Changed status from Advanced Information to Preliminary.<br>Updated Features (for package offering).<br>Updated Ordering Information (Updated part numbers). |
| *B | 223721 | NJY | See ECN | Updated Features (Removed 150 MHz frequency related information).<br>Updated Functional Description (Removed 150 MHz frequency related information).<br>Updated Logic Block Diagram (Splitted Logic Block Diagram into three Logic Block Diagrams).<br>Updated Selection Guide (Removed 150 MHz frequency related information).<br>Updated Functional Overview (Removed 150 MHz frequency related information).<br>Updated Boundary Scan Exit Order (Replaced TBD with values for all packages).<br>Updated Electrical Characteristics (Removed 150 MHz frequency related information, replaced TBD with values for maximum values of $I_{DD}$, $I_{SB1}$, $I_{SB2}$, $I_{SB3}$, $I_{SB4}$ parameters).<br>Updated Capacitance (Replaced TBD with values for all packages).<br>Updated Thermal Resistance (Replaced TBD with values for all packages).<br>Updated Switching Characteristics (Removed 150 MHz frequency related information).<br>Updated Switching Waveforms.<br>Updated Ordering Information (Updated part numbers).<br>Updated Package Diagrams (spec 51-85165 (Changed revision from ** to *A), removed spec 51-85143 and included spec 51-85167 for 209-Ball BGA package, removed spec 51-85115 (corresponding to 119-BGA package)). |
| *C | 235012 | RYQ | See ECN | Minor Change (To match on the spec system and external web). |
| *D | 243572 | NJY | See ECN | Updated Pin Configurations (Updated Figure “165-Ball FBGA (15 × 17 × 1.40 mm) pinout (3 Chip Enable with JTAG)” (Changed ball H2 from $V_{DD}$ to NC), updated Figure “209-ball BGA (14 × 22 × 1.76 mm) pinout” (Changed ball R11 from DQPa to DQPe)).<br>Updated Capacitance (Splitted $C_{IN}$ parameter into $C_{ADDRESS}$, $C_{DATA}$, $C_{CLK}$ parameters and also updated the values). |
| *E | 299511 | SYT | See ECN | Updated Features (Removed 117 MHz frequency related information).<br>Updated Selection Guide (Removed 117 MHz frequency related information).<br>Updated Electrical Characteristics (Removed 117 MHz frequency related information).<br>Updated Thermal Resistance (Changed value of $\Theta_{JA}$ from 16.8 °C/W to 24.63 °C/W, changed value of $\Theta_{JC}$ from 3.3 °C/W to 2.28 °C/W for 100-pin TQFP package).<br>Updated Switching Characteristics (Removed 117 MHz frequency related information).<br>Updated Ordering Information (Updated part numbers (Removed 117 MHz frequency related information, added Pb-free information for 100-pin TQFP, 165-ball FBGA and 209-ball BGA Packages), added comment of “Pb-free BG packages availability” below the Ordering Information). |
| *F | 320197 | PCI | See ECN | Updated Ordering Information (No change in part numbers, removed comment of “Pb-free BG packages availability” below the Ordering Information). |

## Document History Page *(continued)*

| Document Title: CY7C1471V33, 72-Mbit (2 M × 36) Flow-Through SRAM with NoBL™ Architecture<br>Document Number: 38-05288 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| *G | 331513 | PCI | See ECN | Updated Pin Configurations (Address expansion pins/balls in the pinouts for all packages are modified as per JEDEC standard).<br>Updated Pin Definitions (Added Address Expansion pins).<br>Updated Operating Range (Added Industrial Operating Range).<br>Updated Electrical Characteristics (Updated Test Conditions of $V_{OL}$, $V_{OH}$ parameters).<br>Updated Ordering Information (Updated part numbers). |
| *H | 416221 | RXU | See ECN | Changed status from Preliminary to Final.<br>Changed address of Cypress Semiconductor Corporation from “3901 North First Street” to “198 Champion Court”.<br>Updated Features (Removed 100 MHz frequency related information and added 117 MHz frequency related information).<br>Updated Selection Guide (Removed 100 MHz frequency related information and added 117 MHz frequency related information).<br>Updated Electrical Characteristics (Removed 100 MHz frequency related information and added 117 MHz frequency related information, updated Note 14 (Changed $V_{IH} \le V_{DD}$ to $V_{IH} < V_{DD}$), changed description of $I_X$ parameter from Input Load Current except ZZ and MODE to Input Leakage Current except ZZ and MODE, changed minimum value of $I_X$ parameter (corresponding to Input Current of MODE (Input = $V_{SS}$)) from –5 μA to –30 μA, changed maximum value of $I_X$ parameter (corresponding to Input Current of MODE (Input = $V_{DD}$)) from 30 μA to 5 μA, changed minimum value of $I_X$ parameter (corresponding to Input Current of ZZ (Input = $V_{SS}$)) from –30 μA to –5 μA, changed maximum value of $I_X$ parameter (corresponding to Input Current of ZZ (Input = $V_{DD}$)) from 5 μA to 30 μA).<br>Updated Switching Characteristics (Removed 100 MHz frequency related information and added 117 MHz frequency related information).<br>Updated Ordering Information (Updated part numbers, replaced Package Name column with Package Diagram in the Ordering Information table). |
| *I | 472335 | VKN | See ECN | Updated Pin Configurations (Updated Figure “209-ball FBGA (14 × 22 × 1.76 mm) pinout” (Corrected the ball name for H9 to $V_{SS}$ from $V_{SSQ}$)).<br>Updated TAP AC Switching Characteristics (Changed minimum value of $t_{TH}$, $t_{TL}$ parameters from 25 ns to 20 ns, changed maximum value of $t_{TDOV}$ parameters from 5 ns to 10 ns).<br>Updated Maximum Ratings (Added the Maximum Rating for Supply Voltage on $V_{DDQ}$ Relative to GND).<br>Updated Ordering Information (Updated part numbers). |
| *J | 1274732 | VKN / AESA | See ECN | Updated Switching Waveforms (Updated Figure 4 (Corrected typo)). |
| *K | 2898501 | NJY | 03/24/2010 | Updated Ordering Information (Removed inactive part numbers).<br>Updated Package Diagrams. |
| *L | 3034798 | NJY | 09/21/2010 | Added Ordering Code Definitions.<br>Added Acronyms and Units of Measure.<br>Minor edits.<br>Updated to new template. |
| *M | 3357114 | PRIT | 08/29/2011 | Updated Package Diagrams (spec 51-85050 (Changed revision from *C to *D), spec 51-85165 (Changed revision from *B to *C), spec 51-85167 (Changed revision from *A to *B)). |

## Document History Page *(continued)*

| Document Title: CY7C1471V33, 72-Mbit (2 M × 36) Flow-Through SRAM with NoBL™ Architecture<br>Document Number: 38-05288 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| *N | 3633894 | PRIT | 06/01/2012 | Updated Features (Removed CY7C1473V33, CY7C1475V33 related information, removed 165-ball FBGA package, 209-ball FBGA package related information).<br>Updated Functional Description (Removed CY7C1473V33, CY7C1475V33 related information, removed the Note “For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.” and its reference).<br>Updated Selection Guide (Removed 117 MHz frequency related information).<br>Removed Logic Block Diagram – CY7C1473V33.<br>Removed Logic Block Diagram – CY7C1475V33.<br>Updated Pin Configurations (Removed CY7C1473V33, CY7C1475V33 related information, removed 165-ball FBGA package, 209-ball FBGA package related information).<br>Updated Pin Definitions (Removed JTAG related information).<br>Updated Functional Overview (Removed CY7C1473V33, CY7C1475V33 related information).<br>Updated Truth Table (Removed CY7C1473V33, CY7C1475V33 related information).<br>Removed Truth Table for Read/Write (Corresponding to CY7C1473V33, CY7C1475V33).<br>Removed IEEE 1149.1 Serial Boundary Scan (JTAG).<br>Removed TAP Controller State Diagram.<br>Removed TAP Controller Block Diagram.<br>Removed TAP Timing.<br>Removed TAP AC Switching Characteristics.<br>Removed 3.3 V TAP AC Test Conditions.<br>Removed 3.3 V TAP AC Output Load Equivalent.<br>Removed 2.5 V TAP AC Test Conditions.<br>Removed 2.5 V TAP AC Output Load Equivalent.<br>Removed TAP DC Electrical Characteristics and Operating Conditions.<br>Removed Identification Register Definitions.<br>Removed Scan Register Sizes.<br>Removed Identification Codes.<br>Removed Boundary Scan Exit Order (Corresponding to CY7C1471V33, CY7C1473V33, CY7C1475V33).<br>Updated Operating Range (Removed Industrial Temperature Range).<br>Updated Electrical Characteristics (Removed 117 MHz frequency related information).<br>Updated Capacitance (Removed 165-ball FBGA package, 209-ball FBGA package related information).<br>Updated Thermal Resistance (Removed 165-ball FBGA package, 209-ball FBGA package related information).<br>Updated Switching Characteristics (Removed 117 MHz frequency related information).<br>Updated Package Diagrams (Removed 165-ball FBGA package (spec 51-85165), 209-ball FBGA package related information (spec 51-85167)). |
| *O | 3766472 | PRIT | 10/04/2012 | No technical updates.<br>Completing Sunset Review. |
| *P | 3970182 | PRIT | 04/18/2013 | Added Errata. |
| *Q | 4038218 | PRIT | 06/24/2013 | Added Errata Footnotes.<br>Updated to new template. |
| *R | 4146627 | PRIT | 10/04/2013 | Updated Errata. |

## Document History Page *(continued)*

| Document Title: CY7C1471V33, 72-Mbit (2 M × 36) Flow-Through SRAM with NoBL™ Architecture<br>Document Number: 38-05288 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| *S | 4539205 | PRIT | 10/15/2014 | Updated Package Diagrams:<br>spec 51-85050 – Changed revision from *D to *E.<br>Completing Sunset Review. |
| *T | 4572829 | PRIT | 11/18/2014 | Added related documentation hyperlink in page 1. |

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