EVALUATION KIT AVAILABLE

MAXIM

3¾ Digit DMM Circuit

General Description

The MAX133 and MAX134 are integrating A/D converters for 3¾ digit multimeters and data acquisition systems such as data loggers and weigh scales. The A/D's internal resolution is ±40,000 counts. An extra digit is supplied as a guard digit to allow autozero or tare of a 4000 count displayed reading to 1/10 of a displayed count. The conversion time is 50ms.

The MAX133 and MAX134 differ only in their microprocessor interface. The MAX133 has a 4 bit multiplexed address/data bus while the MAX134 has 3 separate address lines and a 4 bit bidirectional data bus. Both devices can be used with 4, 8, and 16 bit microprocessors.

When controlled by a microprocessor, the MAX133 and MAX134 can perform auto-ranging measurements from ±400.0mV to ±4000V full scale. External attenuator resistors are required, but range switching is performed by the A/D.

The power supply is typically a 9V battery or ±5V. Operating current is typically 100μA while standby current in only 25μA.

Applications

Digital Panel Meters
Weigh Scales
Data Loggers
Data Acquisition Systems

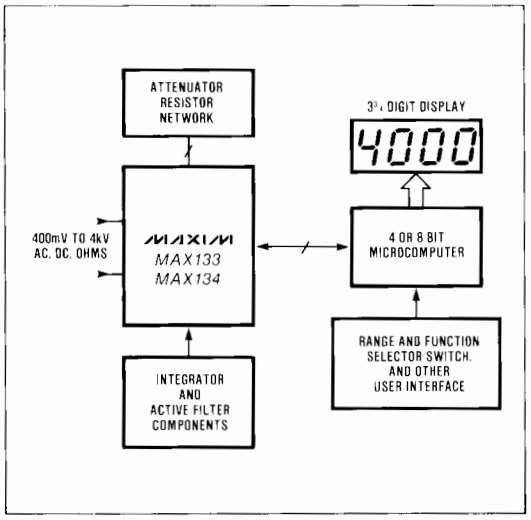
Features

- **40,000 Count Resolution**
- **0.025% Accuracy**
- **20 Conversions per Second**
- **Microprocessor Interface**
- **100μA Operating Supply Current**
- **Low External Component Count**
- **5μV Resolution**
- **Demonstration Kit Available MAX134/DEMO**

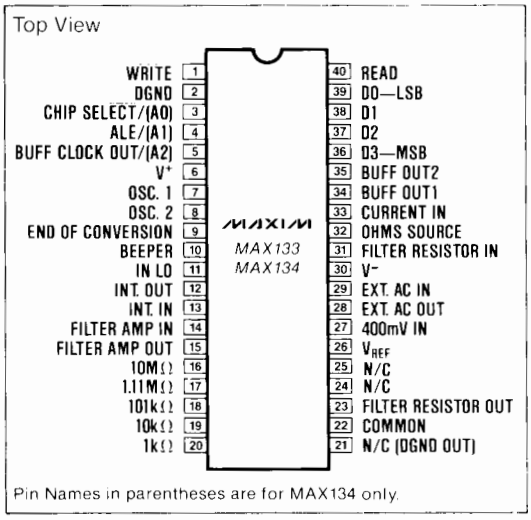
Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX133CPL	0° C to +70° C	40 Lead Plastic DIP
MAX133CQH	0° C to +70° C	44 Lead Plastic Chip Carrier
MAX133C/D	0° C to +70° C	Dice
MAX133EPL	-40° C to +85° C	40 Lead Plastic DIP
MAX133EQH	-40° C to +85° C	44 Lead Plastic Chip Carrier
MAX134CPL	0° C to +70° C	40 Lead Plastic DIP
MAX134CQH	0° C to +70° C	44 Lead Plastic Chip Carrier
MAX134C/D	0° C to +70° C	Dice
MAX134EPL	-40° C to +85° C	40 Lead Plastic DIP
MAX134EQH	-40° C to +85° C	44 Lead Plastic Chip Carrier

Typical Operating Circuit



Pin Configuration



Pin Names in parentheses are for MAX134 only.

3¾ Digit DMM Circuit

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- V^+ to V^- ..... +15V
- V^+ to DGND ..... +6V
- V^- to DGND ..... -9V

Analog Input Voltage (any input) (Note 1) ..... V^+ to V^-

Reference Input Voltage ..... V^+ to V^-
Digital Inputs ..... (DGND - 0.3V) to (V^+ + 0.3V)
Power Dissipation 800mW
Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering 10 sec) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V^+ = 9V, T_A = +25°C, Test Circuit unless otherwise indicated)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
ANALOG					
Zero Input Reading	Read Zero Mode, DC Volts Zero Input Offset Reading will be corrected Digitally in the µP			±5000	Count
ΔZero Input Reading	Difference between 1000VDC Scale, V_{IN} = 0 and 3VDC and Scale, V_{IN} = 0 (Note 3)		2	±2	Count
$I_{10M\Omega}$	Leakage Current into 10MΩ Pin			20	pA
Rollover Error	$V_{IN+} = \lvert V_{IN-} \rvert$ = 3V	-10		+10	Count
Integral Linearity	Best Fit Line 300mVDC Scale Not production tested	10		+10	Count
Differential Nonlinearity	Deviation from ideal Count size Not production tested		0.1	5	Count
Recovery Time	Number of Conversions to settle to within 2 Counts of final reading on 3 VDC Scale after attempting to measure a 2.95V Input on the 300mV Scale. Unfiltered DC Mode Settle to 1 Count		1 2		Conv
CMRR	V_{CM} = ±500mV V_{CM} is (IN LO - Common)		86		dB
Noise	300mVDC Scale Zero Reading Mode Pk-Pk Value exceeded less than 5% of readings		2 2		Count
Zero Reading Drift			0.1		Count/°C
Scale Factor Tempco	300 mVDC scale 0ppm ext Reference			5	ppm/°C
AC TIMING					
t_{AL}	Figure 5, MAX133		130		ns
t_{CC}	Figure 5, MAX133		60		ns
t_{LA}	Figure 5, MAX133		100		ns
t_{LC}	Figure 5, MAX133		1500		ns
t_{LL}	Figure 5, MAX133		20		ns
t_{RD}	Figure 5, MAX133		100		ns
t_{CL}	Figure 5, MAX133		130		ns
t_{DW}	Figure 5, MAX133		100		ns
t_{ACC}	Figure 4, MAX134		3250		ns
t_{EN}	Figure 4, MAX134		80		ns
t_{DF}	Figure 4, MAX134		80		ns
t_{AS}	Figure 4, MAX134		2500		ns
t_{DS}	Figure 4, MAX134		150		ns
t_{DH}	Figure 4, MAX134		75		ns
t_{AH}	Figure 4, MAX134		85		ns

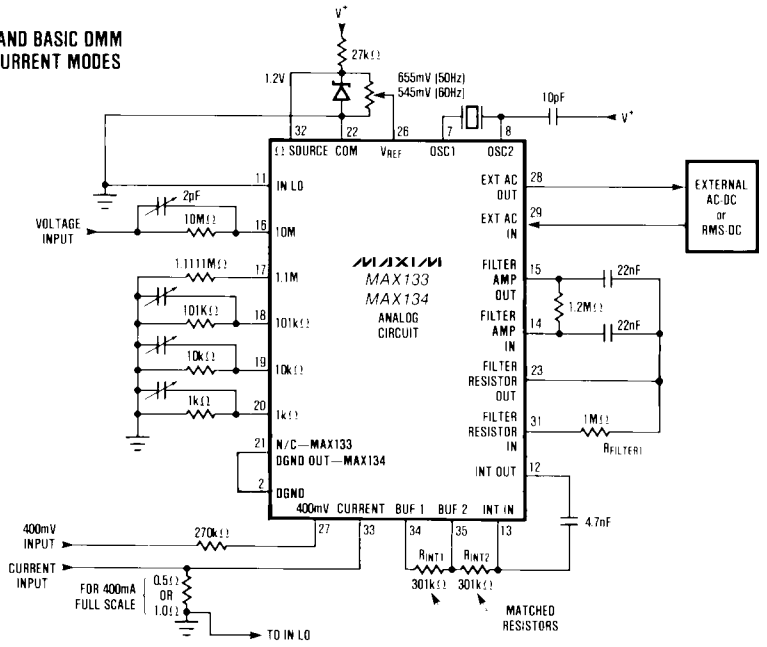
Note 1: Input Voltage may exceed supply voltages, provided the Input Current is limited to ±1mA.
Note 2: Analog performance is specified in counts relative to a 40,000 count full scale; i.e. a spec of 5 counts would correspond to 1/2 of one count on a 3¾ digit meter.
Note 3: This parameter is guaranteed by testing the input bias currents of the input pins 10MΩ and 1.11MΩ.

ELECTRICAL CHARACTERISTICS (continued)

(V^+ = 9V, T_A = +25°C, Test Circuit unless otherwise indicated)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
POWER SUPPLY AND DIGITAL SECTION						
Digital Ground Voltage	DGND	Referenced to V^+ $5\mu A < I_{SINK} < 500\mu A$	-4.5	-5	-5.5	V
Analog COMMON Voltage		(V^+ - Common) 250kΩ between V^+ and COMMON	2.8	3.0	3.3	V
Analog COMMON Sink Impedance		ΔV, I_{COMMON} = 10μA to I_{COMMON} = 2mA		4	20	Ω
Analog Common Source Capability		For $\Delta V_{COMMON} < 0.5V$		1		μA
Tempco of Common				80		ppm/°C
Output High	V_{OH}	D_{0-3}, Data Ready I_{OUT} = -100μA	V^+ - 0.5			V
Output Low	V_{OL}	D_{0-3}, Data Ready I_{OUT} = 400μA			0.4	V
Input High	V_{IH}	D_{0-3}, A_{0-3}, Data Ready, RD, WR	70	45		% (V^+ - DGND)
Input Low	V_{IL}	D_{0-3}, A_{0-3}, Data Ready, RD, WR		1.6	0.8	V
Supply Current	I_{SUPP}			100	250	μA
Sleep Current	I_{SLEEP}			25		μA
Low Battery	V_{LBAT}	Low Battery Flag On	6.3	6.8	7.5	V

TEST CIRCUIT AND BASIC DMM VOLTAGE AND CURRENT MODES



NOTE: Pin Numbers are for the 40 Lead DIP.

3¾ Digit DMM Circuit

System Considerations

The MAX133/134 is intended for use with a microprocessor. The MAX133/134 contains an A/D and auxilliary circuitry such as attenuator range switches, a piezoelectric beeper driver, an active filter, a low battery detector, and both analog and digital power supplies; but it does not include any display drive capability. The MAX133/134 reduces the component count and system cost by minimizing the external components required for the analog portion of the system, but does not restrict final product features by including autoranging or other digital control functions. The MAX133/134 is intended to work as the analog front end of a microprocessor, with the features of the end product being determined by the microprocessor software. Table 1 shows how the execution of several typical functions is partitioned between the MAX133/134 and the microprocessor.

The MAX133/134 provides all of the logic and counters for control of the conversion sequence, and the external microprocessor does not have to perform any critical timing or complex control of the MAX133/134. The MAX133/134 has range switches for a 5 decade attenuator which uses external resistors, and has additional mode-selection circuitry for performing voltage, current, AC or DC, ohms, and continuity measurements. The 5 decade attenuator and mode-selection circuitry is controlled by an external microprocessor via control bits written into the MAX133/134.

The MAX133/134 has normal mode rejection of line frequency of at least 80dB on the voltage ranges; the microprocessor selects rejection of either 50Hz or 60Hz by setting a MAX133/134 control bit. A two pole active filter can also be turned on by the microprocessor, adding about 40 dB normal mode rejection above 50Hz. See the "Digital Interface" section for details on which functions can be controlled by the external microprocessor.

The basic blocks of the MAX133/134 are

- A/D section
- Input Range Switching
- Ohms Circuitry
- Active Filter
- Power Supply, Common, Low Battery Detector
- Oscillator and Beeper Driver
- Digital Interface

A/D Section

The A/D uses a "residue multiplication" conversion scheme to provide a full ±40,000 count resolution reading every 50 milliseconds, while still providing the excellent noise performance and power line normal mode rejection associated with integrating A/Ds. See "Conversion Method and Timing" below for details of the conversion method. All timing and A/D conversion phase control is performed by the MAX133/134 without microprocessor intervention. The A/D section will perform a non-zero-corrected conversion every 50 milliseconds (20 conversions per second).

The microprocessor must periodically direct the MAX133/134 to perform a read zero conversion, which also takes 50 milliseconds. This read zero conversion is a conversion performed with IN LO internally

Table 1. Coordination of the MAX133/134 and the Microprocessor

FUNCTION	MAX133/134 ACTION	MICROPROCESSOR ACTION
Autoranging	Contains the attenuator control switches. Selects 400mV to 4000V ranges as directed by the microprocessor.	Detects overload and commands the MAX133/134 to select the next higher range. Range switching hysteresis and manual range selection is controlled by the microprocessor.
Zero Reading (system offset correction)	Internally shorts the A/D inputs and performs a measurement of system offset when directed by the microprocessor.	Periodically commands the MAX133/134 to perform a zero reading. Subtracts this zero reading from normal readings to correct for the internal offset of the MAX133/134.
Range/Function Selection	Selects Ohms/Current/ AC-DC/Voltage/Continuity as directed by the microprocessor.	Maintains the user interface, and directs the MAX133/134 to select the desired range.
Display of Readings	Max 133/134 provides raw, non-zero-corrected data to microprocessor.	The microprocessor performs zero correction and any gain correction or scaling that is desired. The microprocessor then displays the information, using either its own display driver capability or an external display driver.
Value added DMM features such as display hold, peak hold, either manual range selection or autoranging, peak reading hold, min/max display, thermocouple linearization, etc.	Performs conversions as directed by the microprocessor, returning the A/D results to the microprocessor.	Uses the MAX133/134 conversion results and software routines to provide a multitude of product features.
Digital panel meter features such as zero and span adjustment, high/low limit alarms, display in engineering units, etc.	Performs conversions and range selection as directed by the microprocessor.	Takes the MAX133/134 readings, performs zero offset and scale corrections, then displays the results. The microprocessor also performs such functions as high/low limit alarms.

shorted to IN HI, and the result of this zero conversion must be subtracted (by the microprocessor) from normal measurements to obtain a zero-corrected reading. The zero correction that must be subtracted is determined by the MAX133/134's internal offsets. Since these offsets are relatively slow changing, zero conversion readings need only be taken often enough to track long term drifts and temperature changes. The zero conversion reading will change slightly with a change in common mode input voltage or reference voltage, and a new zero conversion reading should be taken if either of these change.

In ratiometric ohms measurement the reference voltage will change significantly as the value of the unknown resistor varies. To reduce the errors caused by the system offset the MAX133/134 "chops" the input buffer and integrator. The "chop" consists of a reversal of the input transistors during the conversion cycle. The timing of this chop is such that in the R/2 or ohms measurement mode, the system offset is almost completely nulled out if the X2 mode is not selected. Even if the X2 mode is selected, the system offset does not exceed 5000 counts on any range. Since the internal full scale range of the MAX133/134 is greater than ±49,000 counts, at least ±40,000 counts of resolution are available after zero offset correction.

Each conversion result is latched into a Conversion Register which can be read by the microprocessor. The data format is nines complement BCD (a zero reading is 00000, a -1 reading is 99999, a -25000 reading is 75000). The nines complement form is the most convenient BCD format since the addition of the nines complement of a number is equivalent to subtracting that number. See "Software Notes" for simple BCD to binary conversion algorithms.

The last digit of conversion is used for digital autozero and is usually not displayed. Note that each count of the least significant digit of the MAX133/134 output corresponds to 1/10 of a count if a 4000 count full scale display is used. For current ranges with a voltage drop of only 200mV, the measured reading can be multiplied by two by using the X2 ("times 2") function of the MAX133/134. The X2 function reduces the R_{INT} resistor value by a factor of two during the Integrate phase. With the X2 range, a 200mV input voltage will result in a full scale, 4000.0 measured reading. Alternatively, the normal 400mV range can be used, with the multiplication by two being done by the microprocessor digitally. In this case, each count of the least significant digit is 1/5 of a displayed count. A 100mV full scale voltage drop can be achieved by using both the MAX133/134 X2 range and a digital times 2 multiplication in the microprocessor.

Each of the 20 conversions per second has a Zero Integrator phase to ensure rapid recovery from overload, and the MAX133/134 will recover to within 2 counts one conversion after an overload of 10 times full scale when the onboard active filter is not used.

Input Range Switching

In voltage measurement ranges other than 400mV, voltages are applied to the pin labeled 10MΩ through a 10MΩ resistor. By selecting the proper shunt resistors (1.1MΩ through 1KΩ) the input voltage will be attenuated to a 400mV range. The input attenuator switch section includes analog switches to switch both the input current and to sense the voltage on the shunt resistor. Other input switching functions select between the output of the input attenuator and the voltage developed across the current sensing resistors during current measurement. See Figure 1.

The 5pA input bias current of the MAX133/134 might result in unacceptable errors with a 10MΩ input resistor on the 400mV scale, so a separate pin with a 100kΩ to 1MΩ input resistor is used for the 400mV scale. The 10MΩ resistor used on the higher voltage ranges does not cause appreciable error since the input leakage current is shunted to ground through the 1.11MΩ to 1kΩ attenuator shunt resistors.

To avoid errors that might occur through coupling of high frequency, high voltage signals from the input of the attenuator to the low level 400mV and Current inputs, these two inputs have 10kΩ switches which connect them to Common whenever they are not selected.

The input section also includes switches to allow an external AC-DC converter to be inserted into the signal path. Figure 10 shows a typical average-sensing RMS-calibrated AC-DC converter.

Ohms and Diode Measurement

The input attenuator resistors are also used as reference resistors in the ohms mode. Note that the 10MΩ resistor must be externally paralleled with the other resistors to get exactly 1MΩ, 100kΩ, etc. The ohms source buffer input is usually connected directly to the external bandgap reference or to another 1.25V source. In the 4kΩ through 40MΩ ranges there will be a total of 1.25V across the series combination of reference resistor, unknown resistor, and the input protection network; and the maximum voltage across the unknown resistor at full scale will be less than 400mV. On the 400Ω range, the ohms voltage source is a diode connected to V^+ through a 2kΩ p-channel switch. With a 3V Common voltage, this supplies approximately 2.2V across the series combination of reference resistor, unknown resistor, and input protection network. This higher voltage is used on the 400Ω range to compensate for the decrease in reference voltage caused by the input protection network. The MAX133/134 are designed to operate with PTC protection resistors of 2kΩ or less.

The voltage across the reference resistor is used as the reference voltage for the A/D when in the ohms mode, and the differential voltage between IN LO and IN HI is the input signal. The integration period is 500 counts, independent of the 50/60Hz control bit setting.

3¾ Digit DMM Circuit

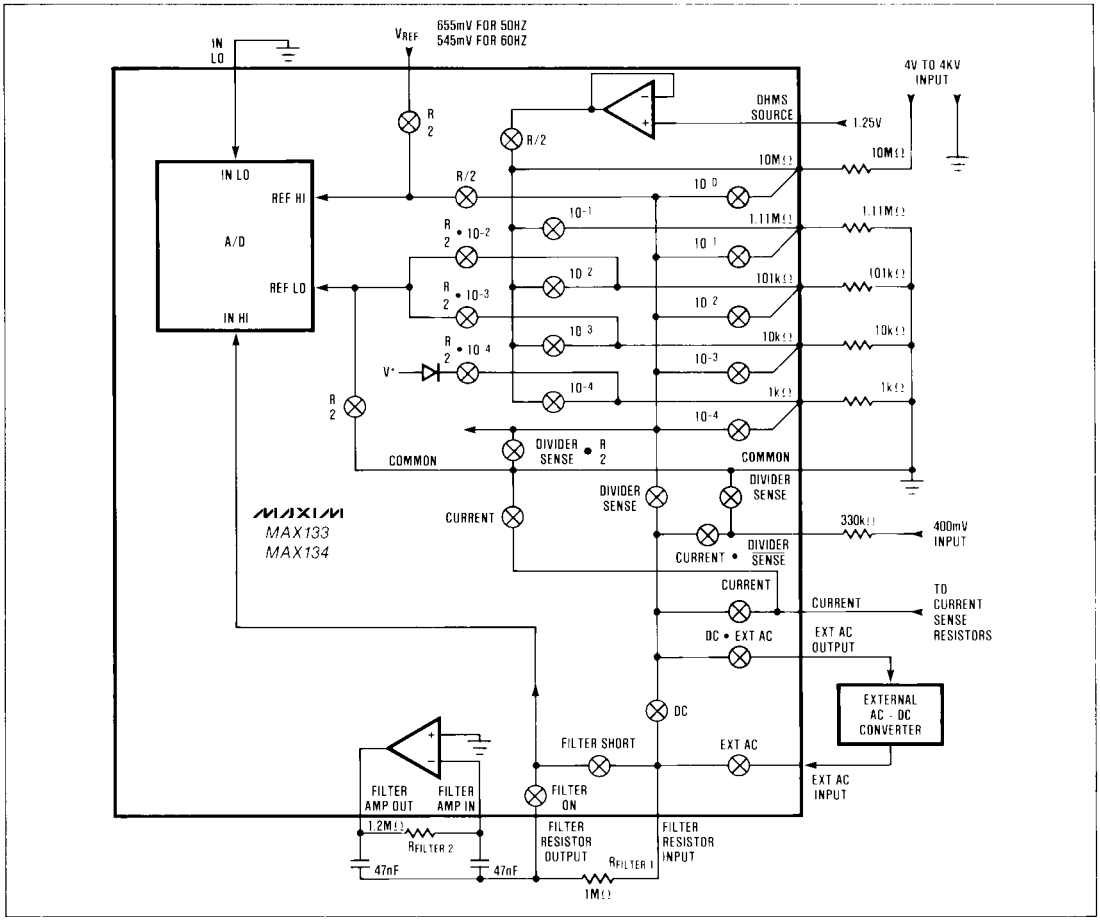


Figure 1. MAX133/134 Input Section

The digital output code is

$$50000 \times \frac{R_{UNKNOWN}}{R_{REF}}$$

with a maximum non-zero-corrected output code of ±49,520 and a maximum zero reading of 5000.

A 1kΩ reference resistor is used for the 400Ω full scale, a 10kΩ reference for a 4kΩ full scale, etc. A 10MΩ reference resistor is used for both the 4MΩ full scale and the 40MΩ full scale. To get the correct results in the ohms measurement or R/2 mode, the conversion result must be multiplied by two either digitally by the microprocessor or by using the X2 range, except on the 40MΩ scale. The 40MΩ range has the same reference resistor as the 4MΩ range but a times 10 scale factor is obtained by not multiplying by 2, and by activating the ÷5 function. If the times 2 multiplication is performed by the microprocessor, the Read Zero offset of the MAX133/134 in the ohms mode will be just a few counts, and will be nearly independent of the value of the unknown resistor being measured. If the MAX133/134 X2 mode is used to multiply by 2, then frequent Read Zero readings should be taken, since the read zero offset is inversely proportional to the reference voltage, and the reference voltage varies as the resistance of the unknown resistor varies.

Since the input protection PTC resistor shown in Figure 2 reduces the reference and input voltage, particularly on the 400Ω scale, the PTC resistance should be as low as is possible while maintaining the desired level of protection. Greater than 2kΩ PTC resistance will increase the noise level of measurements on the 400Ω range.

Since the MAX133/134 does not use a reference capacitor, the only limit on the response time in the ohms mode is the active filter. Even when the active filter is turned off, $R_{FILTER1}$ is still connected, and the input voltage must charge the filter capacitors. This will generally be noticed only on the 4MΩ and 40MΩ ranges.

A diode test range can be implemented by simply connecting to V^+ the PTC used for input protection in the ohms ranges. The PTC then delivers approximately 1mA of current to the diode. The diode voltage can be measured either on the standard 4V scale, or on the 400mV scale with the ÷5 function activated to result in a 2V full scale. As always, the latched continuity circuit is active, and it will latch whenever the input voltage goes below approximately 100mV. The microprocessor can also test the measured voltage at the end of each conversion if a more precise detection of continuity threshold is desired.

Active Filter

The 2 pole active filter circuit is shown in Figure 3. The op amp's offset has no effect on the DC accuracy since the op amp is only AC coupled and the DC signal path is only through the passive 1MΩ resistor. Note that the active filter will limit the speed of response of the MAX133/134 to input voltage changes, and for that reason it may be desirable to disconnect the input filter during autoranging. Since the source impedance at the filter input varies with the input attenuator selected, the response time will be slower on the 4V range.

Oscillator and Beeper Driver

The MAX133/134 is designed to operate with a 32768Hz tuning fork crystal similar to the Statek CX-1V, using only one external capacitor and no external resistors. If desired, the MAX133/134's OSC1 pin can be driven externally.

The 32kHz clock is used internally as the clock for the sequence and measurement counters. The 32kHz clock is also divided down to 2048Hz and 4096Hz for driving a beeper. The beeper output swings from V^+ to V^- and can directly drive piezoelectric beepers. Two control bits set by the microprocessor select the frequency (2048 or 4096 Hz) of the beeper and turn it on or off. Since the beeper is controlled by the microprocessor, it can be used for both continuity indication and for an audible operator feedback signal for peak hold or range changes.

Power Supply: Common, Digital Ground, Low Battery Detector

Both the MAX133 and MAX134 can operate from either a nominal 9V battery or a ±5V supply. The maximum power supply current in DC voltage and DC current modes is 250μA, with a typical operating current of 100μA.

Analog Common is derived from a zener and is nominally 3.0V below V^+. For lowest cost applications the Common voltage, with a tempco of 80ppm/°C, may be usable as a reference. In most applications, a bandgap reference will be connected to Common, with a pullup resistor to V^+, and a voltage divider connected across the bandgap reference to generate the 545mV (60Hz operation) or 655 (50 Hz operation) reference voltage. In a battery powered meter, the Analog Common pin is used as the system ground reference point.

The MAX133 and MAX134 also generate a Digital Ground voltage, which is nominally 5V below V^+,

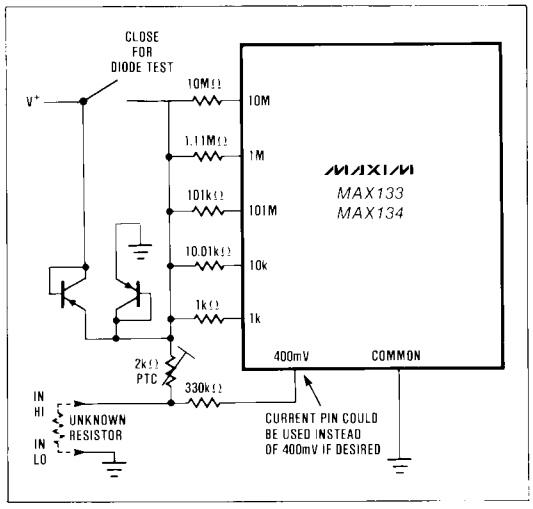


Figure 2. Ohms Mode and Diode Test

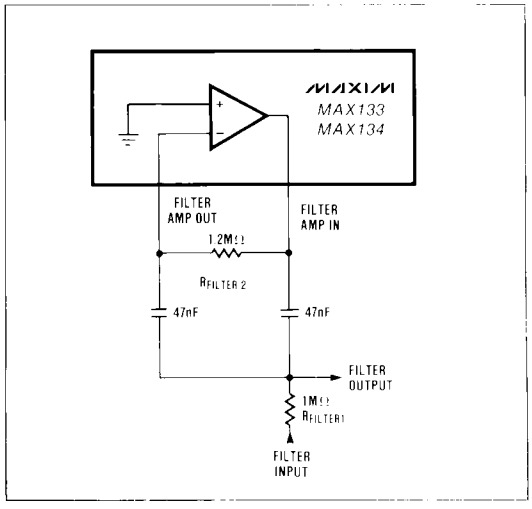


Figure 3. Active Filter

3¾ Digit DMM Circuit

and which will remain in the range of 5V ±10% while sinking 5μA to 500μA. The DGND generator has substantial current sinking capability, but can easily be pulled to a more negative voltage since the current sourcing capability is only 1 μA typical. The MAX133 internally connects the Digital Ground generator to the DGND pin. Normally the MAX133 is powered by a 9V battery and the Ground, V⁻, or V_{SS} pin of the microprocessor is connected to the MAX133 DGND pin.

The MAX134 connects the DGND voltage generator to the pin, DGND Out, and the MAX134 DGND pin is an input only. For use with 9V batteries, externally connect the MAX134 DGND Out pin to the MAX134 DGND pin. For use with external ±5V power supplies, connect the DGND pin to ground, V⁺ to +5V and V⁻ to -5V.

The MAX133/134 has an onboard low battery detect circuit that will indicate when the battery voltage is approaching the minimum operating voltage of the MAX133/134, which is approximately 6.8V.

Digital Interface

The MAX133 and MAX134 differ only in their digital interface. The MAX133 has a multiplexed address and bidirectional data bus, while the MAX134 has 3 separate address lines in addition to a bidirectional data bus. In both products, the data bus has 4 bits, allowing the use of the MAX133/134 with both 4 bit and 8 bit microprocessors.

MAX134 Digital Interface

The digital interface between the MAX134 and the controlling microprocessor is via a 4 bit bidirectional bus, D0-D3. In addition to the 4 data bus lines, there are 3 address lines and 2 control signals: A0-A2, WR, and RD.

The three address lines, A0-A2 select one of 5 control registers. When WR goes low, data will be written from the bus into the MAX134 control register addressed by A0-A2. When RD is low, the MAX134 will drive the bidirectional bus, placing on it the data contained in the results or status register addressed by the address inputs A0-A2. Figure 4 shows typical read and write sequences.

Digital Interface, MAX133

The MAX133 uses only 7 lines to interface with the microprocessor. The microprocessor first selects the register to be read or written to by placing the address of the register onto the 4 bit multiplexed address/data bus. The microprocessor then pulses the Address Latch Enable (ALE) line high to latch the register address into the MAX133. To read the selected register, the microprocessor then drives the Read line low, and the MAX133 places the register data onto the data bus. To write to the selected register the address is latched as described above, then the microprocessor places the data onto the bus and then pulses the Write line low. The MAX133 latches the data into the data into the selected register on the rising edge of Write. See Figure 5. The Chip Select (CS) line must be low to enable either the RD or WR lines, but ALE is not gated by CS.

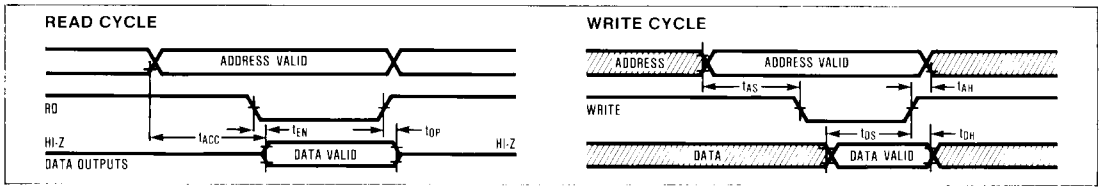


Figure 4. MAX134 Read and Write Sequence

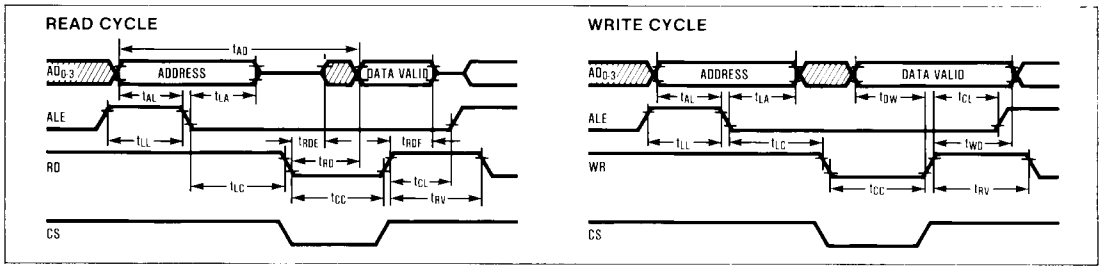


Figure 5. MAX133 Read and Write Sequence

Digital Interface, MAX133 and MAX134

In most cases, the EOC signal will be either monitored by an I/O pin, or it will drive an Interrupt pin on the microprocessor. In battery powered systems, it may be desirable to put the microprocessor into a sleep or standby mode until EOC goes high. The microprocessor then performs any required data processing and display updates, then reenters the sleep mode. This conserves battery power since the microprocessor power consumption is minimized.

The data that has been latched in the MAX133/134 control registers does not immediately affect operation. The input registers are double buffered, and the control bits take effect during the 21st clock cycle after EOC goes high. In the hold mode, the double buffered registers are transparent, and any updates to the registers take effect immediately, as do any changes made during the one clock cycle period at the end of each conversion during which the second rank of buffers are being updated.

Description of Output Bits

The data format is nines complement BCD. For example:

MEASUREMENT RESULT	BCD DATA
+40000	40000
—	—
+00100	00100
—	—
+00001	00001
+00000	00000
(there is NO -00000)	
-00001	99999
—	—
-00100	99900
—	—
-40000	60000

The Latched Continuity bit will be high if the input voltage has gone below the continuity threshold of approximately 100mV since the last time the register was read. Each time this register (Register 5) is read, the continuity latch is reset.

The Low Battery bit is high whenever the battery voltage is below the low battery detect voltage.

The $\overline{\text{Holding}}$ bit is low whenever the MAX133/134 is in the hold state.

Description of Control Bits

Hold. A 1 in Hold will stop conversions at the end of the next conversion. If the MAX133/134 is in the Hold mode, a conversion will start on the next clock cycle after Hold is set to 0. The oscillator continues to run and all circuitry is active during the Hold mode.

High Frequency. A 1 in the High Frequency bit will select 4096Hz as the beeper frequency. A 0 will select 2048Hz.

Beeper On. A 1 turns on the beeper driver.

Sleep. A 1 in Sleep puts the MAX133/134 into the standby or sleep mode. The Common voltage buffer is turned off and the internal analog circuits are turned off, but the DGND circuitry is still active. The oscillator continues to run. Current consumption is reduced to 25μA. Several conversions must be performed after exiting the Sleep mode before full conversion accuracy is obtained.

10-0 through 10-4. These bits control the attenuator network switches. The 10-0 bit selects the 10MΩ input without activating any shunt resistors. This is an alternate 400mV input. The 10-1 bit activates the 10:1 attenuation by selecting the 10MΩ input and connecting the 1.111MΩ shunt. Similarly, 10-2, 10-3, and 10-4 bits selects input attenuation factors of 100, 1000, and 10,000 respectively. In the ohms mode these bits set the resistance range.

Table 2: Register Map of Output Data From the MAX133/134 to the Microprocessor

ADDRESS OR REGISTER NUMBER	REGISTER NAME	REGISTER CONTENTS			
0	Ones	Conversion Result BCD data for least significant digit (The undisplayed digit used for digital autozero)			
1	Tens	BCD data of Conversion Result (Least significant displayed digit)			
2	Hundreds	BCD Data of Conversion Result			
3	Thousands	BCD Data of Conversion Result			
4	10 Thousands	BCD Data of Conversion Result			
5	Status	D3 Always 1	D2 Latched Continuity	D1 Holding	D0 Low Battery

3¾ Digit DMM Circuit

Table 3. Register Map of Input Data From the Microprocessor to the MAX133/134

ADDRESS OR REGISTER NUMBER	D3	D2	D1	D0
0	Hold	High Frequency	Beeper ON	Sleep
1	10-0	Filter Short	÷5	50Hz
2	10-4	10-3	10-2	10-1
3	DC	Ext AC	Divider Sense	Ohms R/2
4	Current	X2	Read Zero	Filter On

BIT SET	VOLTAGE RANGE	OHMS RANGE
10-0	400mV	4MΩ and 40MΩ
10-1	4V	400kΩ
10-2	40V	40kΩ
10-3	400V	4kΩ
10-4	4000V	400Ω

NOTE: The divider sense bit must also be set to enable the 10-0 through 10-4 bits.

50Hz. When set to 1 the integration period for voltage measurement is one cycle of the 50Hz power mains (655 clock cycles). When 0, the integration period is one 60Hz power line cycle (545 clock cycles).

X2. Setting the bit to 1 activates the MAX133/134 "times 2" function. When X2 is active, R_{INT2} only is used as the integrator resistor during the integration phase. R_{INT1} and R_{INT2} in series are used as the integration resistor for all deintegration phases and for the integration phase when X2 is 0. If $R_{INT1} = R_{INT2}$ then setting the X2 bit doubles the digital output for a given input voltage.

÷5. When this bit is set to a 1 the integration period is reduced by a factor of 5. This reduces the digital output code by a factor of 5, and allows a higher input voltage to be used. The full scale input voltage is multiplied by 5 when this bit is set, but caution should be used to make sure that the 2μA maximum recommended integrator output current is not exceeded, or the MAX133/134 linearity will be degraded.

Ohms or R/2. Setting this bit to a 1 selects the ohms measurement mode. See "Ohms and Diode Measurement" section above. Set the Divider Sense to 0 for ohms measurements.

Read Zero. Setting this bit to a 1 causes the next conversion to be a Read Zero conversion. A read zero conversion is performed with In Hi and In Lo internally shorted, and the reference selected by the other control bits is used. The read zero conversion result is proportional to the internal offsets of the MAX133/134, and this result should be subtracted from other measurements to get zero-corrected readings.

Filter On and Filter Short. These bits control the active filter. See Figures 1 and 3.

FILTER ON	FILTER SHORT	FUNCTION
1	0	Normal filter on condition
1	1	Filter on, $R_{FILTER1}$ is bypassed. Use this bit combination to compensate for the higher source impedance of the 4V range.
0	1	Bypasses the Filter.
0	0	Invalid combination, do not use.

DC. This bit selects the DC mode when set to 1 and selects the AC mode when it is 0. This bit should also be set for ohms measurement.

External AC. This bit should be set to 1 whenever the AC mode is selected (DC=0).

Divider Sense. This bit, the 10-0 through 10-4, and the Current bits select the input signal source. Divider sense should be 1 whenever the input attenuator is selected. Set Divider Sense to 0 to select the 400mV input.

Current. Set divider sense to 0 and the Current bit to 1 to select the Current input. Note that while this bit and the associated pin are named "Current", the actual input is the voltage drop across an external current sensing resistor.

Component Selection

Integration Resistors

For an accurate times 2 multiplication in the X2 mode, the two R_{INT} resistors must be exactly equal. If the X2 mode is not needed, then connect a 604kΩ R_{INT1} between Buffer Out1 and the integration capacitor C_{INT}, and leave Buffer Out2 open. The value of both R_{INT1} and R_{INT2} is normally 301kΩ for a 545mV or 655mV reference. This sets the integrator output current to 2μA during the Deintegrate phase. resistors proportionately. Do not exceed 8μA integrator current.

Integration Capacitor

The normal value for the integration capacitor is 4.7nF. This value, in combination with the integrator output current and the clock frequency sets the integrator swing to about 3V for the voltage ranges when $R_{INT1} = R_{INT2} = 301k\Omega$ and the clock frequency is 32,768Hz. While the same integrator swing can be achieved with other values of capacitors by changing the value of R_{INT}, lower values of C_{INT} may introduce more noise through increased pickup of noise and 50/60Hz signals. Excessively high values of C_{INT} will also cause noise problems by reducing the integrator swing to unacceptably low values, causing the comparator noise to dominate the conversion errors. Large values of C_{INT} will also cause linearity errors since the settling time of the internal times 10 circuitry is affected by the value of C_{INT}.

The dielectric absorption of the integration capacitor directly affects the integral linearity, and high quality polypropylene capacitors are recommended. Polycarbonate and polystyrene capacitors may give satisfactory performance in less demanding applications, while the fourth choice, polyester (Mylar), will cause about 0.1% integral non-linearity.

Active Filter Components

The RC time constant of the active filter components sets the rolloff frequency of the filter. The effective value of the $R_{FILTER1}$ (Figure 3) is the sum of its value plus the source impedance driving the filter. In the 30V range for example, the effective source impedance is the 101kΩ resistor in the attenuator. In the 3V range, the effective source impedance is 1MΩ. This variable source impedance will alter the filter characteristics somewhat as the different voltage ranges are selected. The effect of the different source impedances can be minimized by increasing the value of the filter resistors while decreasing the value of the filter capacitors proportionately. This, however, will increase the offset error caused by the A/D input leakage current flowing through the filter resistors. For most applications, filter resistor values between 1MΩ and 3MΩ are optimal.

The RC time constant sets the filter rolloff frequency. A low rolloff frequency improves the normal mode rejection, but at the expense of a longer settling time in response to input voltage step changes. Another consideration when an LCD bargraph is used is aliasing. If the bargraph is updated at 20 times per second and there is a 19Hz component in the signal being measured, the beat frequency of 1Hz will appear on the LCD bargraph display. To avoid aliasing effects, the filter time constant is normally set to less than 10Hz. A 3Hz rolloff (RC = 40ms) further reduces the aliasing effects and increases normal mode rejection while still maintaining an acceptable transient response with fast varying signals.

Dielectric absorption in the filter capacitors will create a small, long time constant settling error; therefore polypropylene capacitors are recommended.

Crystal, and Crystal Oscillator Capacitor

The MAX133/134 oscillator is designed to use high Q, low power 32,768Hz crystals such as the Statek CX-1V. The series resistance should be less than 30kΩ.

The oscillator capacitor connected to OSC2 is typically 10pF, but should be adjusted to optimize performance with the chosen crystal. If overtone oscillations are observed, then increase the value of the oscillator capacitor. If on the other hand, the oscillator has start-up problems, then reduce or eliminate the oscillator capacitor. Keep the stray capacitance across the crystal to a minimum since excessive stray capacitance will prevent oscillation.

Attenuator Network

The attenuator network and the associated range selection switches are shown in Figure 1. If the resistance of the internal range selection switches were 0Ω, then the theoretically ideal values for the attenuator network would be 10MΩ, 1.1111MΩ, 101.101kΩ, 10.01kΩ and 1.0001kΩ.

The voltage coefficient of the 10MΩ resistor should be as low as possible, since it will have high voltages applied to it in the 400V and 4,000V ranges. In addition, the temperature coefficients of the various attenuator resistors should be as low as practical since this affects the accuracy of the ohms measurements. The temperature coefficients of the attenuator resistors should track each other since the ratio of the resistor values sets the accuracy of the voltage measurements.

Input Attenuator Compensation Capacitors

The input attenuator is often compensated with low value capacitors to maintain a constant attenuation ratio over a wide bandwith. The value of the compensation capacitors should be as low as practical, otherwise the 10MΩ pin will be driven above V^+ or below V^- when high frequency, high voltage signals are applied to the attenuator input, causing gross conversion errors.

Positive Temperature Coefficient Resistor (PTC)

As shown in Figure 2, a PTC is normally used as part of the protection circuit in the ohms mode. Excessive values of PTC resistance, however, reduce the voltage across the unknown and reference resistors, particularly on the 400Ω range. PTC resistances above 2kΩ will degrade system performance by reducing the signal level on the 400Ω range, thereby increasing the conversion noise. Values above 5kΩ will cause additional error since the voltage drop across the PTC appears at the A/D as a common mode difference between IN HI and Ref LO.

Microprocessors

For low cost 2 chip digital multimeters, 4 bit microprocessors with LCD display drive capability are

3¾ Digit DMM Circuit

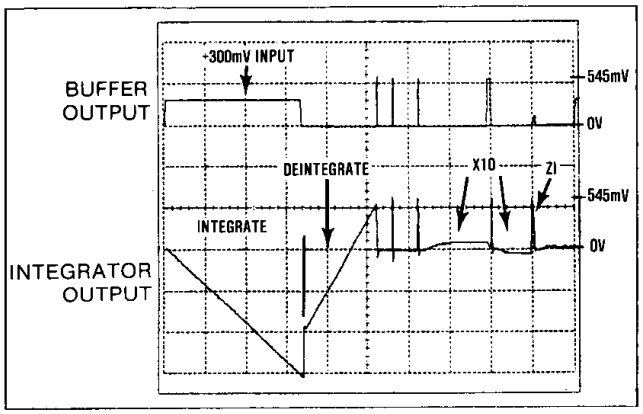


Figure 6. Buffer and Integrator Waveforms with Fullscale Positive Input Voltage

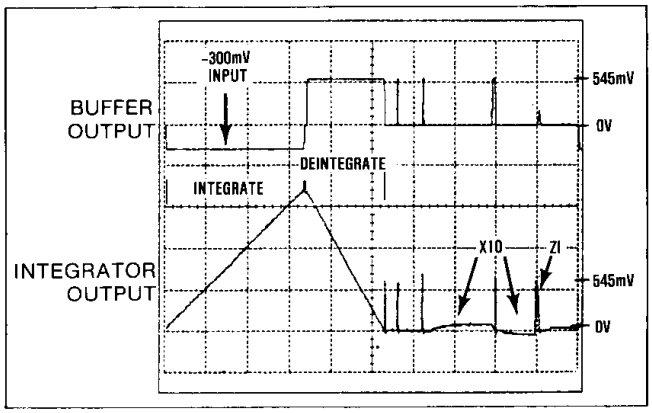


Figure 7. Buffer and Integrator Waveforms with Fullscale Negative Input Voltage

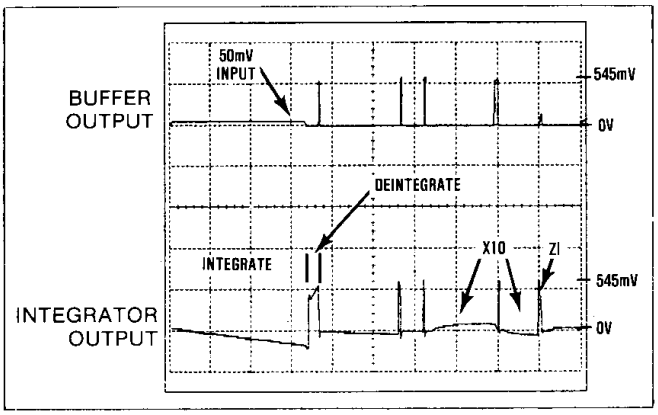


Figure 8. Buffer and Integrator Waveforms with a Small Positive Input Voltage

recommended. Typical 4 bit microprocessor families include the Sharp SM4 and SM5, the NEC μPD75XX family, and the Hitatchi LCD-III and LCD-IV families. If additional calculation power is needed, or if software development costs and time need to be minimized, then 8 bit microcontrollers such as the 8048, 8051 or 6803 should be used.

A/D Conversion Method and Timing

The MAX133/134 uses a "residue multiplication" technique to perform a ±40,000 count conversion in only 1638 clock cycles. Figures 6, 7 and 8 show typical integrator and buffer waveforms for a large positive, a large negative, and a small positive input voltage respectively.

Integration Phase

The unknown signal is integrated by connecting the non-inverting input of the integrator to IN LO, and the buffer input to In Hi. The integration period varies from 100 counts to 655 counts as shown in Table 5. The MAX133/134 is in the Zero Integration phase while in hold, between conversions, and before the start of the integration period.

Table 5. Integration Periods

MODE	INTEGRATION PERIOD (clock cycles)	
Voltage, 60Hz	545	(16.63ms)
Voltage, 50Hz	655	(19.99ms)
Voltage, 60Hz, ÷ 5	109	
Voltage, 50Hz, ÷ 5	131	
Ohms	500	
Ohms, ÷ 5	100	

$$\text{Digital Output Code} = \text{Integration Period} \times 100 \times \frac{V_{IN}}{V_{REF}}$$

where V_{IN} is the differential voltage applied to the A/D's internal In Hi and In LO, and V_{REF} is the differential voltage applied to the A/D's internal Ref Hi and Ref Lo.

First Deintegration Phase

The polarity of the first Deintegrate phase is determined by polarity of the voltage on the integration capacitor at the end of the integration period. Figure 9 shows the MAX133/134 A/D section. Note that no reference capacitor is needed, thereby improving the response time in ohms measurement. Also note that since the non-inverting input of the integrator is connected to Ref Hi for a positive deintegration, the voltage at the integrator output will have a step voltage change equal to the reference voltage.

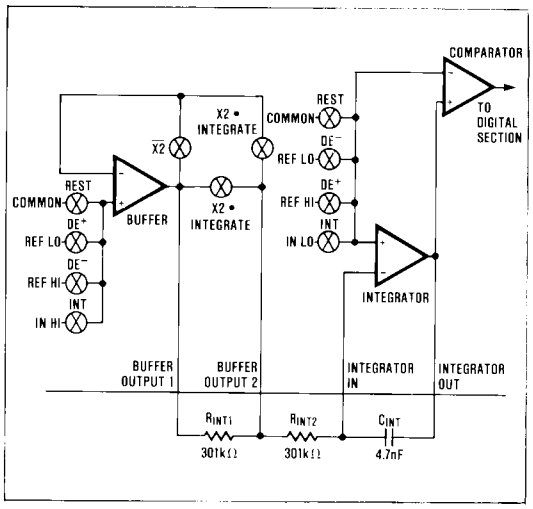


Figure 9. A/D Analog Section.

The first deintegration phase terminates when the comparator detects that the integration capacitor has been discharged. The MAX133/134 then goes into an "Idle" state where both the buffer input and the non-inverting input of the integrator are connected to common. This causes the system offset to be integrated.

Near the end of the maximum allowable deintegration period, the polarity of the voltage on the integration capacitor is again tested and either a positive or negative deintegration cycle occurs.

Times 10 (X10) Phase

When zero crossing is detected at the end of a deintegration phase the deintegration is continued until the next clock cycle. This causes the integrator to overshoot zero crossing slightly, leaving a small residual voltage on the integration capacitor. Any comparator delay causes an additional residual voltage on the integration capacitor. The times 10 phase inverts and multiplies this residual by a factor of 10.

Second Deintegration Phase

The second deintegration phase deintegrates the residual voltage on the integration capacitor that has been inverted and multiplied by 10 in the X10 phase. Note that, since the voltage across the integration capacitor has been multiplied by 10, each clock cycle of deintegration during the second deintegration corresponds to 1/10 of one clock cycle during the first deintegration.

Second X10 and Third Deintegration

The residual voltage left on the integration capacitor after the second deintegrate phase is multiplied by the second X10 phase, and this multiplied residual is deintegrated in the third deintegration phase. Since the residual voltage on the integration capacitor has twice been multiplied by 10, the third deintegration phase has 100 times finer resolution than does the first deintegration phase.

Sequence Counter and Results Counter

The sequencing or timing of the various conversion phases are controlled by a binary sequence counter. This counter counts upward continuously except during the hold mode. Some phases, such as the integration periods, are both started and stopped at preset counts. The deintegration phases are started at predetermined counts, but are terminated when the comparator detects zero crossing at the integrator output.

The results counter accumulates counts during all deintegration phases. It is an up/down BCD counter, with the count direction being determined by the deintegration polarity. The first deintegration phase causes the results counter to count by hundreds. Since the second deintegration phase is deintegrating a residual voltage that has been multiplied by 10, the results counter is incremented or decremented by tens during the second deintegration phase. The results counter is incremented or decremented by ones during the third deintegration phase. The content of the results counter is transferred to the results register at the end of each conversion.

Application Notes

Sleep and Hold Mode

The Hold mode stops the internal sequence counter at the end of the next conversion but does not turn off the oscillator or any analog circuitry. The Hold mode can be used to speed up autoranging — see "Autoranging", below. Dielectric absoption in the integration capacitor will cause the first two or three readings after an extended Hold period to have a lower magnitude than the steady state reading.

The Sleep mode puts the MAX133/134 into a low power quiescent mode by shutting off all analog circuitry except the DGND power supply and the oscillator. A typical use of the Sleep mode is to reduce power consumption by turning off the MAX133/134 if the meter is idle for a long period. A

3¾ Digit DMM Circuit

typical method of detecting when the meter is no longer being used is to detect when the reading stays constant and there are no operator inputs such as range or mode changes for an extended period.

Since the Sleep mode turns off all analog circuitry, the first conversion after coming out of the sleep mode is not valid. It will take several readings before the reading has stabilized to within 1 count.

Input Protection for Digital Multimeters

Figure 2 shows a typical multimeter input circuit for ohms measurement. The positive temperature coefficient (PTC) thermistor normally has a resistance of only 2kΩ, but under overload conditions it limits the fault current since the fault current heats the PTC, thereby increasing its resistance several orders of magnitiude. Protection on the voltage ranges is automatic, since the 10MΩ input resistor will limit the input current to safe limits, even with 4000V applied. Current ranges must be protected with fuses or circuit breakers, and the current sense resistors should be bypassed with diodes to limit the voltage drop across the current sense resistors to no more than 2 diode drops.

External AC-DC Converter

Figure 10 shows a typical half wave external AC-DC converter. This circuit is an average-sensing, RMS-calibrated AC-DC converter. This means that the output is proportional to the average AC value rather than the RMS value, but that the output has been multiplied by the 1.11 to correct for the ratio of the average voltage to the RMS voltage of a sine wave. If desired, a true RMS to DC converter can be connected between Ext AC Out and Ext AC In.

Printed Circuit Board Layout

Since the integrator output makes common mode voltage steps equal to the reference voltage to perform a positive deintegration, any stray capacitance on the integration capacitor will cause errors. Stray capacitive loading on the Buffer output should also be minimized to avoid ringing on the buffer output.

The Integrator In node is particularly sensitive to stray pickup of noise and 50/60Hz, therefore C_{INT} should be located as near as possible to the Integrator In pin.

Minimize capacitance on the node that joins the two R_{INT} resistors since this capacitance sets up an RC time constant that rounds off the edges of the input to the integrator and can cause errors. If the times 2 mode is not used, then connect a single R_{INT1} directly from Buff OUT1 to the Integrator In pin. Locate the R_{INT1} resistor as close as possible to the Integrator In pin since the Buffer Output is a low impedance point while the Integrator In pin is a high impedance point.

Any resistance between the MAX133/134 1kΩ pin and the 1kΩ resistor adds the effective value of the 1kΩ resistor, as does any voltage drop between the 1kΩ resistor and the In Lo pin. These resistances should be minimized and/or the 1kΩ resistor value should be reduced to compensate for the resistance of the printed circuit board connections.

The effective resistance of any current sensing resistors is affected by where the voltage is sensed. Connect In Lo directly to one end of the current sensing resistor to avoid errors caused by voltage drops in the Common traces on the printed circuit board.

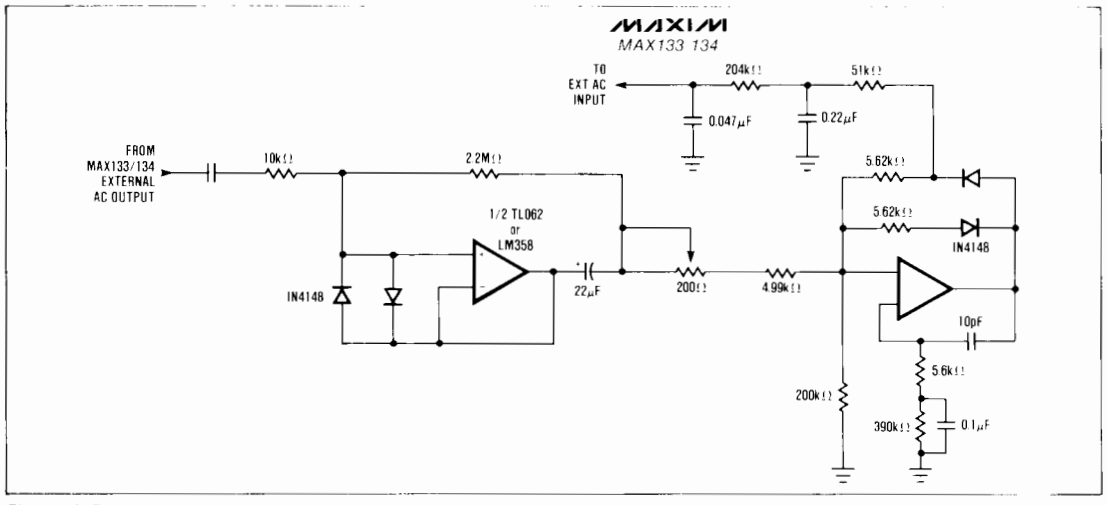


Figure 10. External AC-DC Converter.

Software Notes

Autoranging

The sequence in which the registers are loaded has no effect provided that all registers are loaded before the next end of conversion. Control bits take effect only when the MAX133/134 is in Hold or completes the current conversion. If the MAX133/134 runs continuously, the autoranging sequence will be as shown in Figure 11A. If the MAX133/134 is put into the hold mode during autoranging the autoranging time can be reduced in those cases where several ranges must be tried. See Figure 11B. A simple test that detects most overrange readings is to check if the two most significant digits (Registers 3 and 4) are greater than ±45. A second test of the zero-corrected reading should also be performed to make sure that it is within the desired full scale range.

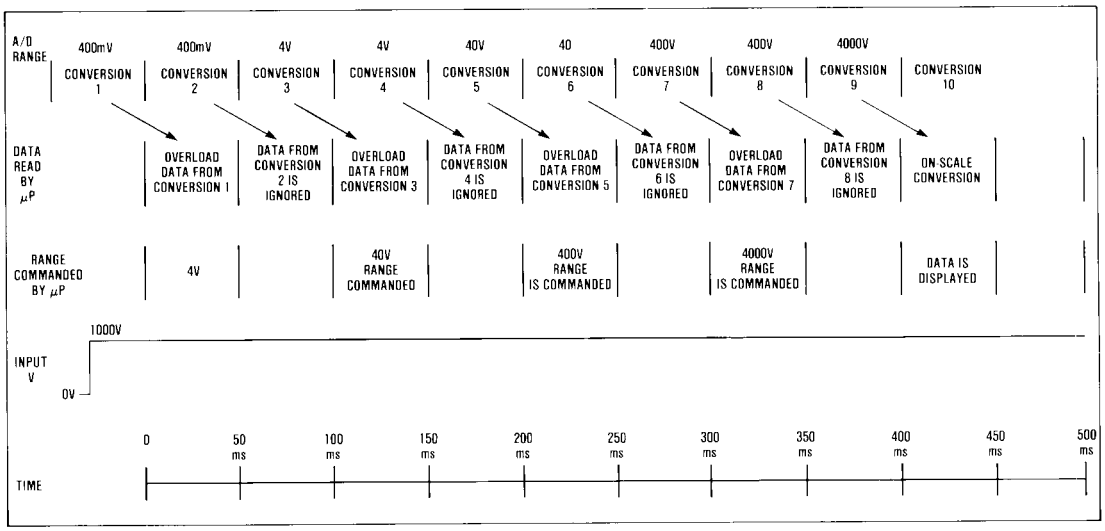


Figure 11a. Autoranging with MAX133/134 Running Continuously

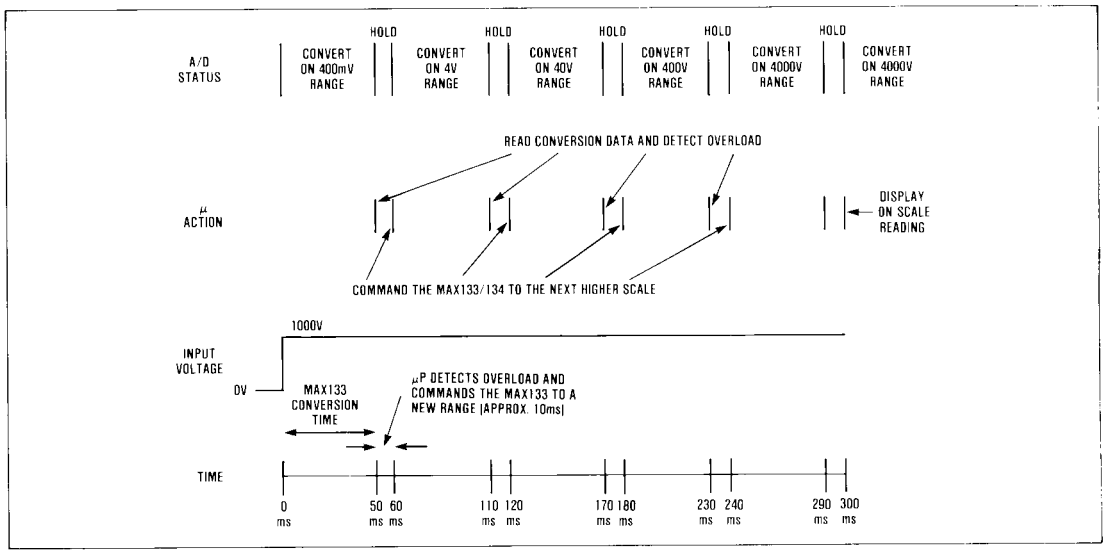


Figure 11b. Autoranging With Hold Between Conversions

3¾ Digit DMM Circuit

Reduction of Conversion Noise by Averaging Readings

The MAX133/134 has approximately ±1 counts of noise. In most cases where only 4000 counts are being displayed, averaging is not required since the noise is only 1/10 of one displayed count. In data acquisition systems where the full resolution is being used, averaging N readings will reduce the noise by a factor of

$\sqrt{N}$.

Since the noise of zero-corrected readings is the RMS sum of the noise of both the Read Zero reading and the normal reading, the Read Zero offset correction should also be averaged if optimum noise performance is desired.

BCD to Binary Conversion

Normally, if only a zero correction or tare correction is to be applied to the output of the MAX133/134, then the conversion result is left in the BCD format. If a scale factor or gain correction is to be made, the result is usually converted to a binary format. Any of the standard BCD to binary conversion algorithms can be used. A simple method of conversion is to read the MAX133/134 conversion result starting with the most significant digit. Put the most significant digit's result into a multi-byte accumulator and multiply it by 10. Then read the next digit's result and add it to the accumulator. Repeat the "multiply-read-add" sequence for all 5 digits.

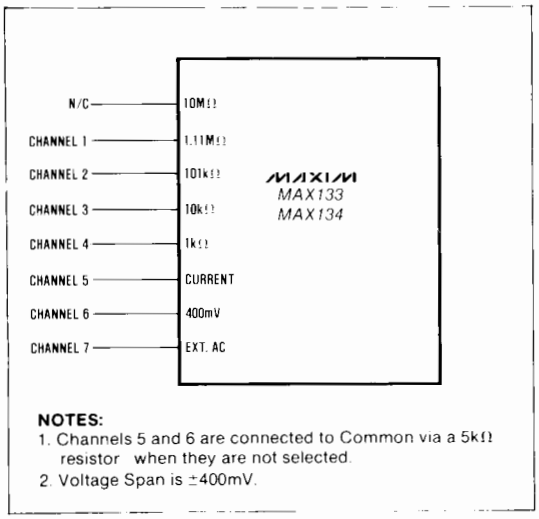
Using the MAX133/134 in Data Acquisition Systems

Using the Input Attenuator Inputs as a Multiplexer

In many data acquisition applications the voltage range is limited, and the 400mV to 4000V attenuator is not needed. In these cases, the input switches can be used as a multiplexer as shown in Figure 12.

Using Non-standard Voltage Ranges

In many data acquisition systems the voltage to be measured may have a full scale range other than 400mV, 4V, etc. For maximum resolution, the full scale range of the MAX133/134 should be adjusted to match the input signal voltage span. This can be done either through attenuation/amplification of the signal to make it match the ±400mV basic span of the MAX133/134, or by adjusting the MAX133/134 voltage span.



NOTES:
1. Channels 5 and 6 are connected to Common via a 5kΩ resistor when they are not selected.
2. Voltage Span is ±400mV.

Figure 12. MAX133/134 Input Section used as a Multiplexer.

Table 5 shows the integration periods of the various conversion modes. These different modes can be used to change the full scale span of the MAX133/134. If for example the reference voltage is 545mV, setting the 50Hz bit changes the integration time to 655 clock cycles and the 400mV full scale range becomes a 545/655 x 400mV = 333mV full scale range. Activating the ÷5 bit increases the full scale span by a factor of 5, while setting the X2 bit decreases the full scale span by a factor of 2 (assuming $R_{INT1} = R_{INT2}$).

In all cases, the values of R_{INT1}, R_{INT2}, and C_{INT} should be chosen so that integrator swing is at least 2V, and integrator current is always less than 3μA both during deintegrate and during integrate with a full scale input voltage. The common mode voltage range of IN Hi and In Lo is from (V^- +1.5V) to (V^+ -1.0V).

Unipolar Operation

Unlike most integrating A/Ds, the MAX133/134 does not have extra non-linearities around zero. This allows the use of the full 80,000 count resolution to measure unipolar signals. All that is needed is a resistive offset network to translate the unipolar signal so that it becomes bipolar. An external zero circuit must be included so that errors in the offset resistor can be

Programming Table for Figure 13

SELECTED CHANNEL	10^{-1}	10^{-2}	10^{-3}	10^{-4}	DIVIDER SENSE	CURRENT	DC	EXT AC
1	1	0	0	0	1	X	1	0
2	0	1	0	0	1	X	1	0
3	0	0	1	0	1	X	1	0
4	0	0	0	1	1	X	1	0
5	0	0	0	0	0	1	1	0
6	0	0	0	0	0	0	1	0
7	0	0	0	0	X	X	0	1

0 = set to 0 1 = set to 1 X = Don't Care

measured and subtracted. Note that the zero correction software is the same as would be used to correct for the internal zero error of the MAX133/134, except that in this case the external zero offset will be nearly 40,000 counts.

Ratiometric Measurements of Load Cell and Strain Gauges

In many weigh scale, pressure transducer, and load cell applications ratiometric measurements are desired. If the reference voltage is referenced to the ground or Common pin, then simply connect the reference voltage to the Ref In pin, connect the voltage to be measured to In Hi and In Lo and perform any of the voltage mode conversions. If, on the other hand, the reference voltage is a differential signal, use the circuit of Figure 13 and select the ohms measurement mode. Note that the non-inverting input of the integrator will be connected to either Ref Lo or REF Hi during deintegration. The integrator swing should be reduced if the integrator output goes within 0.5V of either V^+ or V^-. In no case should either Ref Hi or Ref Lo be lower than (V^- + 1.5V) or higher than (V^+ - 1.0V).

Operation with Clock Frequencies Other Than 32,768Hz

Operation with clock frequencies lower than 32kHz slightly improves the noise performance, while at the same time reducing the reading rate proportionately. With clock frequencies less than 10kHz, leakages during the X10 phase will introduce differential linearity errors at high temperatures.

Clock frequencies higher than 50kHz are not recommended since the X10 period will not completely settle within its allotted time period, causing differential nonlinearity errors. Another potential problem at very high clock frequencies is that, although the comparator delay is a fixed time period, it increases in terms of clock cycles as the clock frequency increases. At very high clock frequencies the residue cannot be fully deintegrated in the allotted number of clock cycles after having been multiplied by 10 in the X10 phase.

When using a clock frequency other than 32,768Hz, change the value of the integration capacitor C_{INT} to keep integrator swing at approximately 2V.

Converting the Times 2 Mode to a ± 40mV Full Scale Range

The sensitivity of the times two mode is increased by the factor

$$\frac{R_{INT1} + R_{INT2}}{R_{INT2}}$$

In the normal DMM aplication $R_{INT1} = R_{INT2}$ and the X2 mode increases the sensitivity of the MAX133/134 by a factor of 2. If the two resistors have a 9 to 1 ratio, the X2 bit will increase the sensitivity of the MAX133/134 by a factor of 10. This can be used to get 1μV resolution on a 40mV scale.

Disabling the Active Filter

Since the signal source impedance in many data acquisition systems is very low, the value of the filter resistors, $R_{FILTER1}$ and $R_{FILTER2}$, can be lowered to reduce the error caused by the leakage current of the A/D flowing through $R_{FILTER1}$. If rapid settling is needed in a multichannel data acquisition system, then the filter should be disabled by leaving the pins Filter Resistor In and Filter Resistor Out open, and shorting Filter Amp Out to Filter Amp In. Do not leave the filter amplifier connection open circuited, since oscillations may occur.

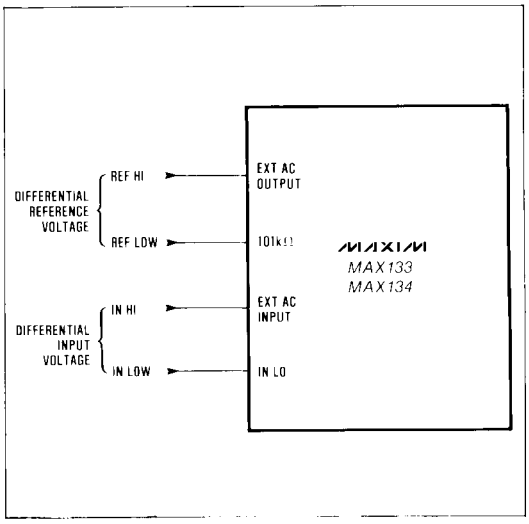


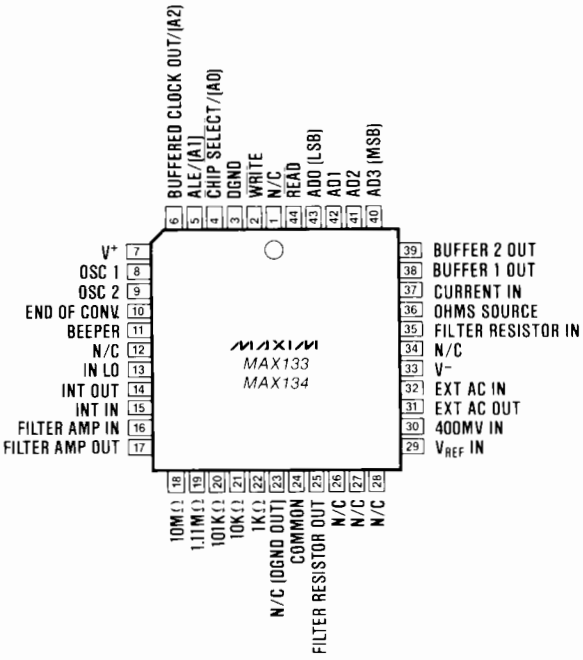
Figure 13. Configuration for Differential Reference Input

BIT PATTERN					
10^{-0} TO 10^{-4}	R/2	DIVIDER SENSE	CURRENT	DC	EXT AC
0	1	1	0	0	1

3¾ Digit DMM Circuit

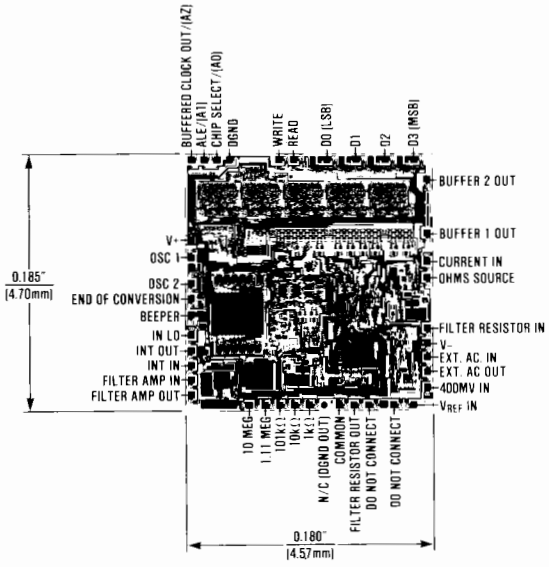
Pin Configuration

TOP VIEW

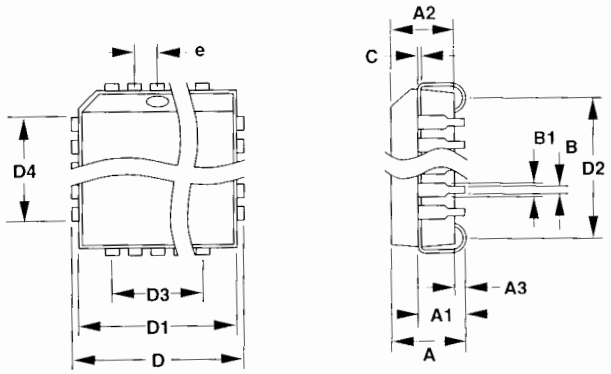


Pin Names in parentheses are for MAX134 only.

Chip Topography



Package Information



PLCC
PLASTIC
LEADED CHIP CARRIER

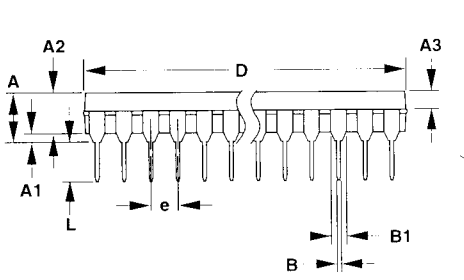
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A1	0.090	0.120	2.29	3.05
A2	0.145	0.156	3.68	3.96
A3	0.020	–	0.51	–
B	0.013	0.021	0.33	0.53
B1	0.026	0.032	0.66	0.81
C	0.009	0.011	0.23	0.28
e	0.050		1.27	

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	20	0.385	0.395	9.78	10.03
D1		0.350	0.356	8.89	9.04
D2		0.290	0.330	7.37	8.38
D3		0.200 REF		5.08 REF	
D	28	0.485	0.495	12.32	12.57
D1		0.450	0.456	11.43	11.58
D2		0.390	0.430	9.91	10.92
D3		0.300 REF		7.62 REF	
D4		0.300	–	7.62	–
D	44	0.685	0.695	17.40	17.65
D1		0.650	0.656	16.51	16.66
D2		0.590	0.630	14.99	16.00
D3		0.500 REF		12.70 REF	
D4		0.470	–	11.94	–
D	68	0.985	0.995	25.02	25.27
D1		0.950	0.958	24.13	24.33
D2		0.890	0.930	22.61	23.62
D3		0.800 REF		20.32 REF	
D4		0.625	–	15.87	–

21-0049B

3 3/4 Digit DMM Circuit

Package Information (continued)



Plastic DIP
PLASTIC
DUAL-IN-LINE
PACKAGE
(0.600 in.)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.020	0.41	0.51
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.050	0.090	1.27	2.29
E	0.600	0.625	15.24	15.88
E1	0.525	0.575	13.34	14.61
e	0.100	–	2.54	–
eA	0.600	–	15.24	–
eB	–	0.700	–	17.78
L	0.120	0.150	3.05	3.81

PKG.	DIM	PINS	INCHES		MILLIMETERS	
			MIN	MAX	MIN	MAX
P	D	24	1.230	1.270	31.24	32.26
P	D	28	1.430	1.470	36.32	37.34
P	D	40	2.025	2.075	51.44	52.71

21-0044A